Technische Universität Darmstadt

Institute of Computer Engineering
Integrated Electronic Systems Lab
Prof. Dr.-Ing. Klaus Hofmann

Bachelor Thesis

Optimization of a High-Voltage, High-Frequency DC-AC Inverter for EL-Lamps

Author : Ferdinand Keil
Supervisor : Dipl.-Ing. Lufei Shen

Start : 22. November 2010
Finish : 22. March 2011

Hiermit erkläre ich, dass ich die vorliegende Arbeit selbstständig und nur mit den nach der Prüfungsordnung der Technischen Universität Darmstadt zulässigen Hilfsmitteln angefertigt habe. Die verwendete Literatur ist im Literaturverzeichnis angegeben. Wörtlich oder sinngemäß übernommene Inhalte habe ich als solche kenntlich gemacht.

Darmstadt, im March 2011

Ferdinand Keil

Herewith I declare, that I have made the presented paper myself and solely with the aid of the means permitted by the examination regulations of the Darmstadt University of Technology. The literature used is indicated in the bibliography. I have indicated literally or correspondingly assumed contents as such.

Darmstadt, March 2011

Ferdinand Keil

Contents

1 Abstract **1**

2 Introduction **3**
2.1 Motivation . . . 3
2.2 Design Specifications . . . 3
2.3 Approaches . . . 4
2.4 Outline . . . 5

3 EL Panels **7**
3.1 Historical Review . . . 7
3.2 Operating Principle . . . 7
3.3 Electrical Model . . . 9
3.3.1 Test Circuit . . . 9
3.3.2 Results . . . 11

4 DC-AC Inverter Topologies **17**
4.1 Switchmode Converter Topologies . . . 17
4.1.1 DC-DC Converter Topologies . . . 17
4.1.2 True DC-AC Inverter Topologies . . . 20
4.2 Resonant Inverter Topologies . . . 23
4.3 Comparison . . . 24
4.4 Conclusion . . . 25

5 Boost converter **27**
5.1 Basic operation . . . 27
5.2 Control Scheme . . . 31
5.3 Power Efficiency . . . 33
5.4 Design Process . . . 35

6 DC-AC Inverter Design **39**
6.1 Boost Converter . . . 39
6.1.1 Control Circuit . . . 39
6.1.2 MOSFET driver . . . 42
6.1.3 MOSFET Selection . . . 43

6.1.4 Diode Selection . . . 43
6.1.5 Simulation . . . 43
6.1.6 Optimization . . . 45
6.2 H-bridge . . . 48
6.2.1 Driver Circuit . . . 49
6.2.2 Part Selection . . . 51
6.2.3 Simulation . . . 51
6.2.4 Optimization . . . 51
6.3 PWM Generation . . . 54
6.3.1 Microcontroller . . . 54
6.3.2 Control Program . . . 55
6.4 Simulation . . . 56
6.5 Evaluation . . . 56

7 Implementation **59**
7.1 Part Selection . . . 59
7.1.1 Passives . . . 60
7.1.2 Diodes . . . 61
7.1.3 Integrated Circuits . . . 61
7.1.4 Transistors . . . 61
7.2 PCB Layout . . . 62
7.3 Experimental Results . . . 62
7.3.1 DC-DC Converter . . . 62
7.3.2 DC-AC Inverter Circuit . . . 64
7.4 Evaluation . . . 66

8 Conclusion and Outlook **69**
8.1 Conclusion . . . 69
8.2 Outlook . . . 70

Bibliography **73**

A Source Code **75**

B Implementation Schematic **81**

C Bill of Materials **83**

List of Tables

3.1 Values measured using the test circuit and calculated parameters. . . 12

4.1 Comparison of the different topologies. 24

5.1 Equations for the design of a boost converter [16]. 36

6.1 Table with design formulas and their results [16]. 41
6.2 Comparison of suitable n-channel MOSFETs for the boost converter. 44
6.3 Comparison of suitable ultra-fast rectifier diodes for the boost converter. 45
6.4 Results from the simulation with different inductance values for *L1*. . 45
6.5 Results from the simulation with different diodes for *D1*. 47
6.6 Results from the simulation with different MOSFETs for *M1*. 48
6.7 Comparison of suitable n-channel MOSFETs for the H-bridge. 52
6.8 Results from the simulation with different diodes for *D1*. 53
6.9 Results from the simulation with different MOSFETs for *M1* and *M2*. 53
6.10 Comparison of the efficiency of the designed boost converter to other existing designs. 58

7.1 Measured results for the DC-AC inverter and different loads. 65
7.2 Comparison of the efficiency of the boost converter part to other existing designs. 66

8.1 Comparison of the design specification to the achieved results. 70

List of Figures

3.1 Cross-section of the layer structure of EL panels [14]. 8
3.2 The process of light emission from excited atoms. 8
3.3 Schematic diagram of a boost converter based on the MC34063 [16]. . 10
3.4 Block diagram of the Atmel ATtiny261 8-bit microcontroller [2]. . . . 11
3.5 Circuit to measure the EL panels electrical properties. 13
3.6 Timing diagram for the waveforms in the test circuit. 14

4.1 DC-DC converter with added H-bridge. 18
4.2 Schematic diagram of the boost converter topology. 18
4.3 Schematic diagram of the flyback converter topology. 20
4.4 Schematic diagram of the push-pull converter topology. 21
4.5 Schematic diagram of the H-bridge converter topology. 22
4.6 Schematic diagram of the Royer converter topology. 23

5.1 Schematic diagram of the boost converter topology. 27
5.2 The two phases of operation of the boost converter. 28
5.3 Timing diagram of the voltage and current waveforms of the boost converter. 29
5.4 Schematic diagram of the boost converter - the control loop is highlighted. 31
5.5 Diagram of a pulse width modulated signal at different duty cycles. . 32

6.1 Schematic diagram of the boost converter circuit as simulated in LTspice. 39
6.2 Representative schematic diagram of the MC34063 [16]. 40
6.3 Schematic diagram of the MOSFET driver circuit as simulated in LTspice. 42
6.4 Schematic diagram of one half-bridge as simulated in LTspice. 48
6.5 Diagram of the bootstrap operation. 49
6.6 Block diagram of the Atmel ATtiny261 8-bit microcontroller [2]. . . . 54
6.7 Flow chart diagram of the control program. 55
6.8 Schematic diagram of the DC-AC inverter circuit as simulated in LTspice. 57
6.9 Output waveform of the simulated DC-AC inverter circuit. 58

7.1 Picture of the circuit board of the implemented circuit. 59
7.2 The PCB artwork for the DC-AC inverter circuit. 63
7.3 Picture of the test circuit used to characterize the implemented circuit. 64

7.4 Output voltage ripple in the real circuit and the simulation. 65
7.5 Ramp-up time in the real circuit and the simulation. 66
7.6 Output current waveform of the DC-AC inverter with an EL panel as load. 67

8.1 Picture of an EL panel glowing while connected to the implemented circuit. 69

B.1 Schematic diagram of the implemented circuit. 82

1 Abstract

The implementation of a high-frequency high-voltage DC-AC converter is investigated in this work and subsequently optimized for low power applications. The aim of the project is to build a low power DC-AC inverter capable of driving EL panels. Several different inverter topologies are introduced and their operating principles are explained. The topologies are compared to each other and the most suitable one is chosen. A circuit employing the boost converter topology and the H-bridge is simulated in SPICE simulation software. The circuit parameters are tuned for highest possible power efficiency with respect to other design requirements. Based on the results a corresponding PCB layout is created and the circuit is fabricated. The system is tested against the load used in simulation and an actual EL lamp. It is compared to a commercial EL panel inverter and achieves superior performance. Several aspects are identified, in which future work has to be done to produce an inverter that can be applied commercially.

2 Introduction

2.1 Motivation

Electroluminescent (EL) panels have been studied for a long time. They have been adopted in various applications such as background illumination for liquid crystal displays (LCD) and emergency lighting. They have an potential as design feature for packaging, advertising and in lifestyle products. Even though EL panel fabrication is well understood, there are still unresolved issues: the high operating voltage of 100V and more, low power efficiency of the driver circuit and audible noise. These problems prevent the use of existing EL technology in some applications, where they would offer unprecedented advantages over common illumination devices. These limitations could be overcome by operating the panels at frequencies above 20kHz and corresponding research is ongoing [14].

Although the results of current research activities have shown that commercially available EL panels can be driven at high frequencies, an inverter capable of providing the required high voltages and high frequencies is still needed. For some new applications the circuit is required to have an adjustable output voltage and frequency, as the EL panel's brightness can be changed by these parameters. At the Institute for Printing Science and Technology at Technische Universität Darmstadt a group of researchers is working on a screen printing process capable of manufacturing EL panels. The printing process is benficial in that it allows the panels to be patterned. It will also be capable to produce the panels fast and at a low cost when finished. To support the research an EL panel DC-AC inverter is needed that offers a variable output voltage and frequency to test and characterize the panels. The circuit would also be used at industry fairs where the institute presents itself regularly.

This work is to design a DC-AC inverter that is robust and can be adapted easily to different types and sizes of EL panels.

2.2 Design Specifications

The EL panel inverter circuit should have an output voltage of a least $120V_{peak-peak}$ and a minimum output frequency of 4000Hz. A compact design is preferrable as is

low audible noise emission. It should be possible to power the circuit from a battery for mobile applications. For battery powered devices high power efficiency typically above 80% is very important.

The design specifications are listed below:

- DC input voltage $\leq$ 12V
- variable AC output voltage $\geq 120V_{peak-peak}$
- variable output frequency $\geq$ 4kHz
- compact design
- low audible noise emission
- high efficiency $\geq$ 80%
- dimming of the EL panel.

2.3 Approaches

At first, the properties of EL panels are further investigated. An electrically equivalent model for an EL lamp manufactured at the Institute of Printing Science and Technology is determined and later used in SPICE simulations of the circuit. Then the most suitable DC-AC inverter topology is discussed and chosen. Several DC-DC and DC-AC converter topologies are introduced and compared to each other. The most suitable is analyzed in detail for a deeper understanding of its operation principles. The power efficiency of the topology is analyzed for later optimization.

After the basic research, the final circuit is designed and simulated. The circuit is optimized for the lowest possible power consumption using SPICE simulation software. The results are evaluated against commercially available circuits. The bill of materials is put together and the choice of components explained. The circuit is entered in a PCB CAD (Computer Aided Design) software and circuit board laid out. The resulting layout is given to PCB manufacturer. The fabricated circuit is thoroughly tested and the measured results are compared to the simulation. The performance of the designed DC-AC inverter circuit is again compared with existing commercially available designs. The results are also compared to the design specifications, to check if these are satisfied.

Finally a conclusion is reached, and an outlook on further research is presented.

2.4 Outline

The design of the DC-AC inverter has been split up in six chapters:

- *Chapter 2* details operating principle and electrically equivalent model of the EL panels.
- *Chapter 3* introduces several different DC-AC inverter topologies and compares them.
- *Chapter 4* discusses the boost converter topology in detail.
- *Chapter 5* documents the design of the DC-AC inverter and the optimization of its sub-circuits.
- *Chapter 6* covers the implementation of the designed circuit and the PCB layout.
- At last, *Chapter 7* draws conclusions and offers an outlook for future work.

3 EL Panels

In this chapter, the physical background of EL panels is given, and the electrical model derived from measurements in the lab is explained.

3.1 Historical Review

1907	First scientific notion on electroluminescence.
1936	Discovery of high field electroluminescence.
1950	Discovery of transparent conducting films leads to first EL panels.
1950 - 1960s	Basic research on EL powder devices.

The first mentioning of the process, that Georges Destriau later named electroluminescence, came from Captain Henry Joseph Round, when he was conducting experiments on silicon carbide detectors in 1907 [3]. Destriau then discovered high-field electroluminescence in 1936. His setup consisted of ZnS phosphor powder embedded in an isolator between two electrodes, to which he applied a high AC voltage. The phosphor started emitting light, and Destriau coined the name electroluminescence for this effect. Due to the lack of transparent electrically conducting devices, the discovery was of no use till the 1950s, when SnO2 conductive films were first developed. In the 1950s and 1960s, ongoing research on the topic of EL powder devices led to the first commercial products such as night-lights or background lighting for instrument panels [8, 18]. The research finally led to the first thin-film EL structures in 1960 by Vlasenko and Popkov. These solved the problems that till then used powder based devices had: poor illumination and short lifetime.

3.2 Operating Principle

EL panels consist of at least five layers as shown in Figure 3.1. Additional layers for robustness might be added. The first layer is a transparent plastic film or glass covered with a layer of conducting material forming the first electrode. The electrode is followed by the phosphor that later illuminates the panel. In screen-printed EL panels and other AC powder EL devices the phosphor consists of suitable doped

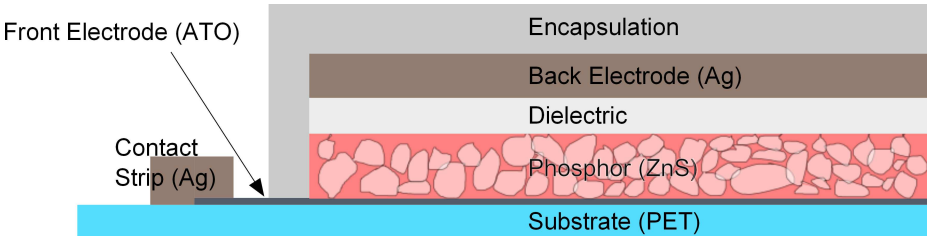


Figure 3.1: Cross-section of the layer structure of EL panels [14].

ZnS grains embedded in an isolating dielectric [8]. On top of the phosphor layer, a dielectric layer is placed to avoid catastrophic dielectric breakdown. The last layer is a transparent electrode allowing the emitted light to shine through. Now the capacitive setup is complete, and the panel can be contacted at the edge of the electrode layers. To add robustness against environmental influences such as humidity, a protective layer is placed on top of the lamp.

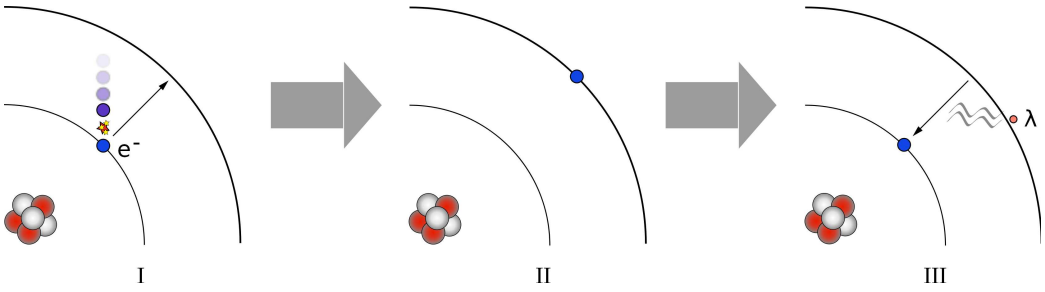


Figure 3.2: The process of light emission from excited atoms.

When a strong electric field of at least $10^6 - 10^7 \mathrm{V/m}$ is applied the phosphor layer starts emitting light [8]. The mechanism behind this emission is as following.

The ZnS (zinc sulfide) and CuxS (copper sulfide) in the phosphor grains form heterojunctions. The CuxS precipitates embedded in the phosphor form conducting needles. When the eletric field is strong enough, tunneling of holes from one end of the needles and electrons of the other is induced. The electrons gain cinetic speeds and exite luminous centers through the impact-excitation mechanism (see Figure 3.2 phase I and II). The excited electrons make radiative transitions falling back to ground thus realizing light emission (see Figure 3.2 phase III) [8].

3.3 Electrical Model

The EL panel as seen from the driving circuit is mainly a capacitance. It can be described in good approximation as capacitance with a series and parallel resistance. The parallel resistance is typically in the range of $4M\Omega/cm^2$ [1].

3.3.1 Test Circuit

To determine the variables of the EL lamps electrical model through measurements with an actual lamp, a prototype of the inverter circuit was built. Several features of the planned inverter were already integrated and tested in the prototype. The circuit consisted of three blocks:

- a DC-DC converter
- a high voltage H-bridge
- a microcontroller with supporting circuitry controlling the H-bridge.

The DC-DC converter outputs a voltage well above the input voltage. This high voltage is then fed to the H-bridge circuit. The H-bridge circuit consists of a controller and four high-voltage MOSFETs. Its output is connected directly to the EL lamps input. The microcontroller switches the H-bridge to create a voltage swing at the output that is twice the input voltage of the bridge circuit. e.g. an input of 12V is converted to 60V by the converter and leads to a $120V_{peak-peak}$ rectangular output voltage at the H-bridge. The circuit was built using readily available and common components. These three building blocks will be explained in detail in three seperate paragraphs.

DC-DC converter

As for the DC-DC converter a simple boost-converter topology was chosen. The industry standard MC34063 control circuit was chosen as the main component for its availability and extensive documentation. The basic schematic diagram of a boost converter based on the MC34063 is shown in Figure 3.3. Because of the high output voltage requirement the control circuit is connected to a high voltage mosfet through a push-pull driver stage. All component values were chosen after the requirements mentioned in the MC34063s datasheet and application notes [15, 16].

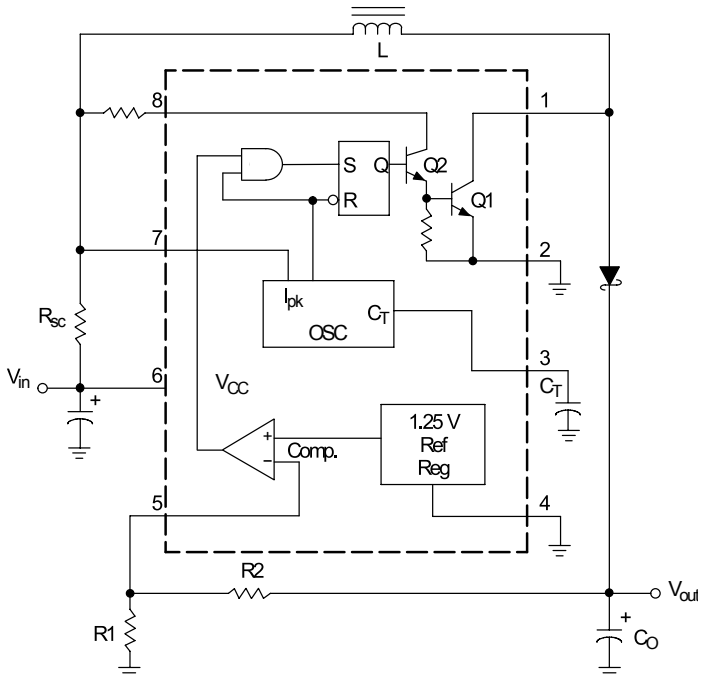


Figure 3.3: Schematic diagram of a boost converter based on the MC34063 [16].

High-voltage H-bridge

For the sake of simplicity an H-bridge using two n-channel MOSFETs per half-bridge was chosen. To be able to control these through the TTL output signals of the microcontroller an special half-bridge driver circuit was needed. The IR2101 was chosen because of its low price point and wide distribution in the industry. The circuit integrates a bootstrap circuit to drive the upper n-channel mosfet in each half-bridge. The values for the supporting components were determined by the device's application note.

Microcontroller

As for the microcontroller part an ATMEL AVR device was chosen. The ATtiny26 and ATtiny261 are especially useful for controlling H-bridges as for their many high-speed and high-precision pulse width modulation (PWM, see Section 5.2) channels. This enables the use of PWM for the creation of arbitrary output waveforms such as sinusoidal ones.

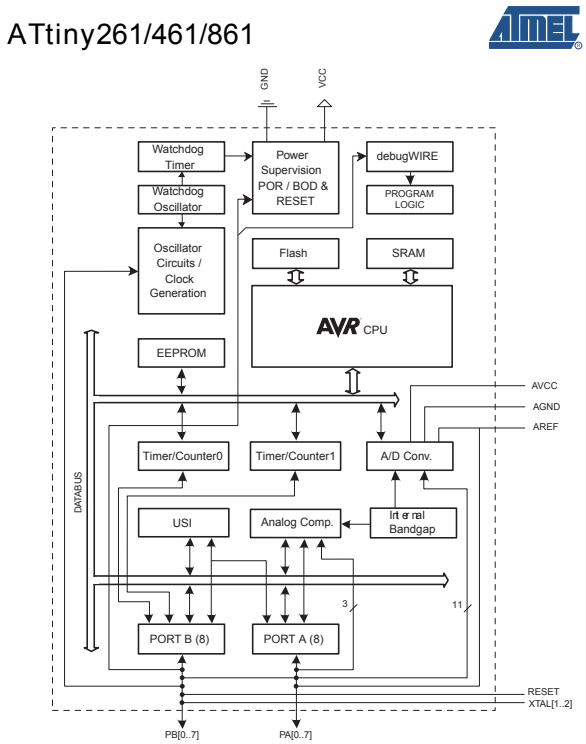


Figure 3.4: Block diagram of the Atmel ATtiny261 8-bit microcontroller [2].

3.3.2 Results

To determine the electrical properties of the EL lamp the setup illustrated in Figure 3.5 was used.

The EL lamp was connected to an AC voltage source with a shunt resistor in series. The AC voltage was of rectangular shape. The voltage across the resistor was measured and recorded with the oscilloscope on channel 1. Knowing the fixed resistance of the shunt resistor the current flowing through it could be calculated from the measured voltage with Ohms law:

$$U = RI. \tag{3.1}$$

The output voltage and frequency of the AC voltage source was sweeped from 20V to 100V and 1kHz to 32kHz. This corresponds to the estimated operating range of the EL lamp.

The voltage across the resistor over time was recorded by the oscilloscope as digital image and raw data.Even though the characteristics of the EL lamp can be approx-

$\mathbf{V_{hv}}$/V	**f**/Hz	$\mathbf{V_{min}}$/V	$\mathbf{V_{max}}$/V	$\mathbf{V_{p-p}}$/V	τ/s	**C**/F	$\mathbf{R_{ser}}/\Omega$	$\mathbf{R_{par}}/\Omega$
20	980	-0,20	19,80	20,00	3,04E-06	15,20E-09	102,02	20528,64
20	1960	-0,80	19,80	20,60	2,98E-06	14,90E-09	102,02	4976,64
20	3922	-0,40	19,80	20,20	3,04E-06	15,20E-09	102,02	10160,64
20	7843	-0,80	19,60	20,40	3,06E-06	15,30E-09	104,08	4976,64
20	15683	-0,80	19,60	20,40	2,96E-06	14,80E-09	104,08	4976,64
20	31369	-1,60	19,20	20,80	2,97E-06	14,86E-09	108,33	2384,64
40	980	-0,40	39,20	39,60	2,94E-06	14,70E-09	104,08	20528,64
40	1960	-1,20	38,80	40,00	3,01E-06	15,05E-09	106,19	6704,64
40	3921	-1,20	38,80	40,00	2,99E-06	14,95E-09	106,19	6704,64
40	7842	-1,20	38,40	39,60	2,98E-06	14,90E-09	108,33	6704,64
40	15682	-1,60	38,40	40,00	2,78E-06	13,90E-09	108,33	4976,64
40	31366	-2,40	37,60	40,00	2,80E-06	14,02E-09	112,77	3248,64
60	981	-0,80	58,80	59,60	3,05E-06	15,24E-09	104,08	15344,64
60	1961	-0,80	58,80	59,60	3,01E-06	15,06E-09	104,08	15344,64
60	3923	-1,20	58,80	60,00	2,95E-06	14,76E-09	104,08	10160,64
60	7846	-2,00	59,60	61,60	3,00E-06	15,00E-09	101,34	6013,44
60	15688	-2,40	58,40	60,80	2,98E-06	14,88E-09	105,48	4976,64
60	31380	-3,60	58,80	62,40	2,87E-06	14,36E-09	104,08	3248,64
80	980	-1,60	76,80	78,40	2,78E-06	13,90E-09	108,33	10160,64
80	1961	-1,60	76,80	78,40	2,73E-06	13,66E-09	108,33	10160,64
80	3922	-1,60	76,80	78,40	2,71E-06	13,54E-09	108,33	10160,64
80	7842	-2,40	76,80	79,20	2,72E-06	13,62E-09	108,33	6704,64
80	15688	-2,40	76,80	79,20	2,72E-06	13,62E-09	108,33	6704,64
80	31383	-4,80	76,00	80,80	2,62E-06	13,10E-09	110,53	3248,64
100	980	-1,60	96,00	97,60	2,50E-06	12,50E-09	108,33	12752,64
100	1962	-0,80	95,20	96,00	2,17E-06	10,84E-09	110,08	25712,64
100	3922	-1,60	94,40	96,00	2,20E-06	10,98E-09	111,86	12752,64
100	7843	-1,60	93,60	95,20	2,27E-06	11,36E-09	113,68	12752,64
100	15684	-4,00	93,60	97,60	2,18E-06	10,90E-09	113,68	4976,64
100	31389	-4,80	91,20	96,00	2,12E-06	10,62E-09	119,30	4112,64

Table 3.1: Values measured using the test circuit and calculated parameters.

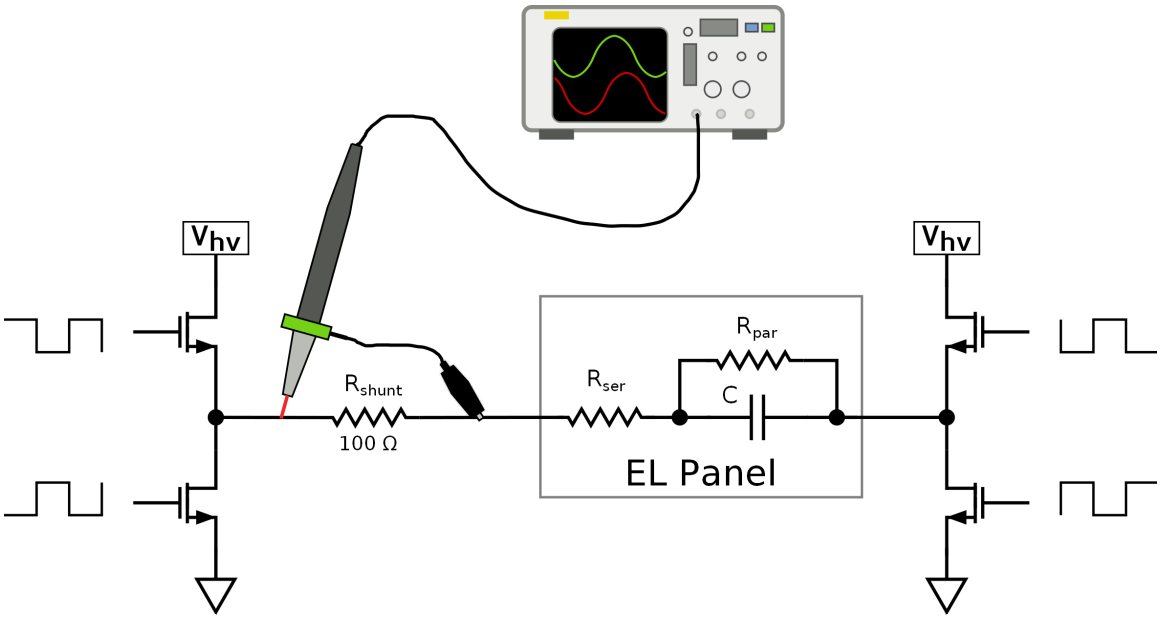


Figure 3.5: Circuit to measure the EL panels electrical properties.

imated by a simple capacitator, a more complex model was used here. As shown in Figure 3.5 the model consists of a capacitator with a series and a parallel resistance. These value needed to be determined to get a realistic model for simulation purposes.

Figure 3.6 shows the waveforms of the voltage across the capacitator, the voltage output from the voltage source and the current through the shunt resistor.

At the beginning V_{AC} is at $+V_{hv}$ and a current $I_{R,shunt}$ flows through Rshunt. At point T_1 the current reaches zero as the voltage across the capacitor equals that of the voltage source. The current flowing through the parallel resistance is not shown in the diagram but was taken into account, when the values for the model were calculated from the measured data. The current $I_{R,shunt}$ stays zero from T_1 to T_2. At T_2 the output voltage of the voltage source is reverted resulting a steep voltage change seen from the resistor. As the capacitor is still charged to $+V_{hv}$ the voltage differential across the left side of the shunt resistor and the right side of the series resistor is now:

$$+V_{hv} - (-V_{hv}) = 2V_{hv}. \tag{3.2}$$

The current flowing through the resistor is limited by its resistance as Ohms law states:

$$I = V/R \tag{3.3}$$

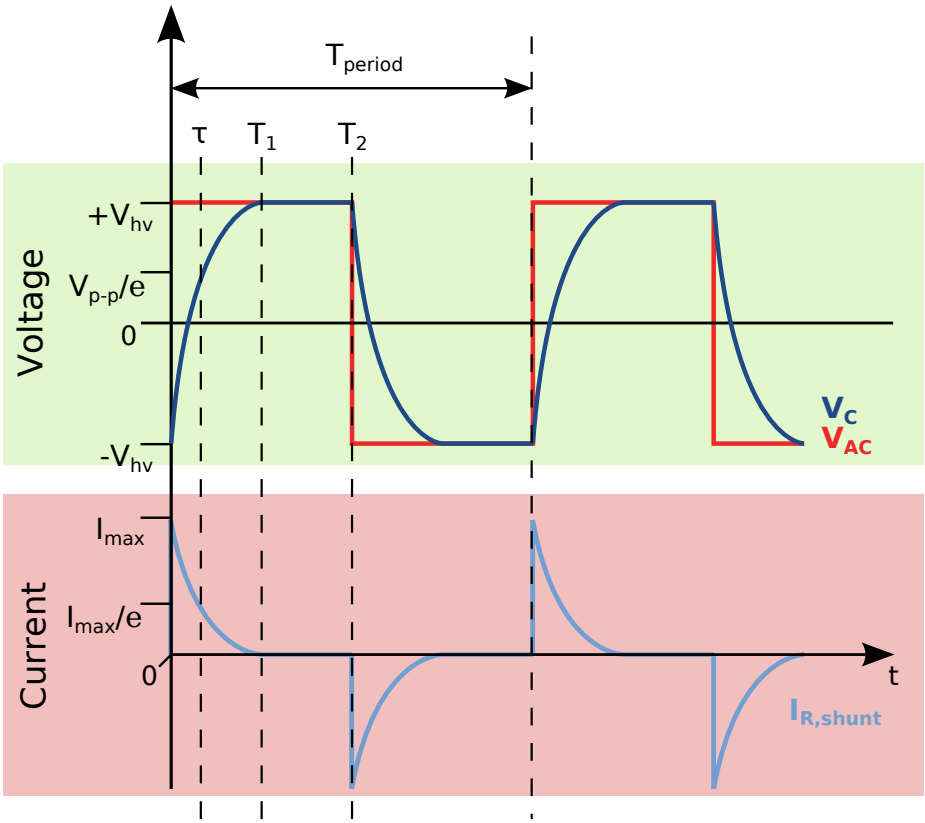


Figure 3.6: Timing diagram for the waveforms in the test circuit.

with R being:

$$R = R_{ser} + R_{shunt}. \tag{3.4}$$

To calculate R_{ser} the maximum voltage across R_{shunt} is measured in order to get the maximum current. As the voltage across the resistor is known R_{ser} can be calculated:

$$\begin{aligned} I_{max} &= V_{R,shunt}/R_{shunt} && (3.5)\\ V_{R,shunt-R,ser} &= I_{max}(R_{ser} + R_{shunt}) && (3.6)\\ V_{R,shunt-R,ser} &= 2V_{hv} && (3.7)\\ \Longrightarrow R_{ser} &= \frac{2V_{hv}}{I_{max}} - R_{shunt} && (3.8) \end{aligned}$$

The maximum current was extracted from the measured data and R_{ser} calculated with the results shown in Table 3.1. For all meausurements the value for R_{ser} is about

100Ω. As Table 3.1 shows, the values for R_{ser} change with the voltage and frequency. That leads to the conclusion, that the EL panel is a non-linear device. A single value for R_{ser} can not derived from the measured data, for simulation the actual data from the table has to be used with interpolation between the recorded points.

Knowing the value for R_{ser} the capacitance of C is to be determined next. Therefore advantage will be taken from R_{shunt}, R_{ser} and C forming a simple RC circuit with a time constant τ given by:

$$\tau = (R_{shunt} + R_{ser})C \qquad \text{source: [4].} \tag{3.9}$$

The time constant is the time required for the voltage across the capacitor to reach 63% or $1/e$ of the applied voltage. This voltage can not be measured directly in this case. As the voltage across the capacitor and the current flowing through the series resistance are proportional to each other the current measurement can be used to determine τ. The point is marked as τ in Figure 3.6 also showing the relation between $I_{R,shunt}$ and V_C ($I_{R,shunt}$ equals $I_{R,ser}$). For each measurement taken the time τ was calculated from the raw data. The results are in Table 3.1. Using Equation 3.9 and the known values for R_{ser} and R_{shunt} the capacitance C was calculated. As can be seen from the results the value changed substantially with the applied voltage and frequency. The EL panels capacitance therefore is non-linear. One has to take the values from Table 3.1 for accurate results.

The last value in the model to be determined is the resistance of R_{par}. As mentioned before current still flows through R_{shunt}, R_{ser} and R_{par} when the capacitor is fully charged because of the voltage diffential between them. The size of this current is proportional to the sum of the resistances as given by Ohms law:

$$I_q = V_{hv}/(R_{shunt} + R_{ser} + R_{par}). \tag{3.10}$$

I_q could be extracted from the measured data by searching for the lowest voltage across the resistor R_{shunt} (given that the rising edge of the current waveform was triggered). Applying Equation 3.10 gives the results in Table 3.1. This factor also shows a non-linear behaviour.

All values for the electrically equivalent model of the EL lamp are now determined and will be used in the simulation of the circuit implementation.

4 DC-AC Inverter Topologies

In this part the different DC-AC converter topologies are discussed. After that they are compared to the requirements of the EL lamp inverter and the most appropriate one is chosen. All of these topologies have in common that they can generate a high AC output voltage from a lower DC input.

4.1 Switchmode Converter Topologies

As the word switchmode implies these topologies rely on a switching element. Therefore the component used has to be either switched fully on or off. In theory it is possible to build a switchmode inverter using almost any switching element. However given the high switching frequencies and the need to optimize the efficiency of these inverters, nearly all modern switchmode topologies rely on semi-conductor components such as bipolar junction transistors, MOSFETs, IGBTs or thyristors. The low on-resistance of modern MOSFETs make it possible to built inverter circuits up to over 90% efficiency. These topologies can be divided in two groups by their output: true DC-AC inverter topologies and DC-DC converter topologies with an added H-bridge. The latter employ an H-bridge connected to the output of a DC-DC converter to generate AC current, while the former outputs AC current directly.

4.1.1 DC-DC Converter Topologies

The two DC-DC converter topologies qualified for the provided application are the the boost converter topology and the flyback converter topology. The boost converter along with the buck converter is one of the most basic DC-DC converter topologies and can be adjusted easily to specific needs.

These two topologies can only output DC current and therefore need addiontional circuitry to create the required AC current. For this application the H-bridge (see Figure 4.1) is the most suitable, as it can effectively reverse the polarities on its outputs and therefore create a peak-to-peak voltage of twice the input voltage. The H-bridge also offers the possibility to create sinusoidal output when controlled with puls width modulated signals and filtered with a low pass filter.

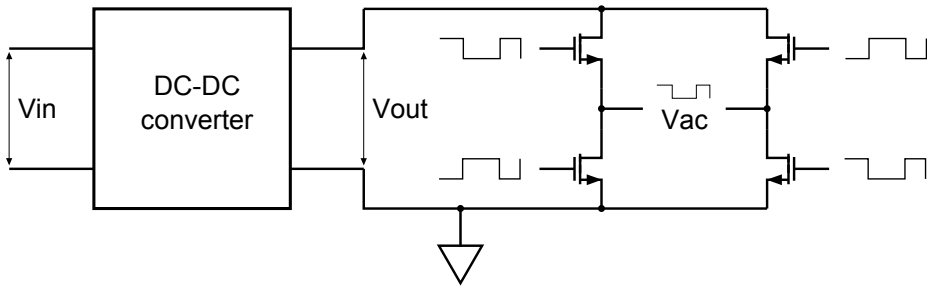


Figure 4.1: DC-DC converter with added H-bridge.

Boost Converter

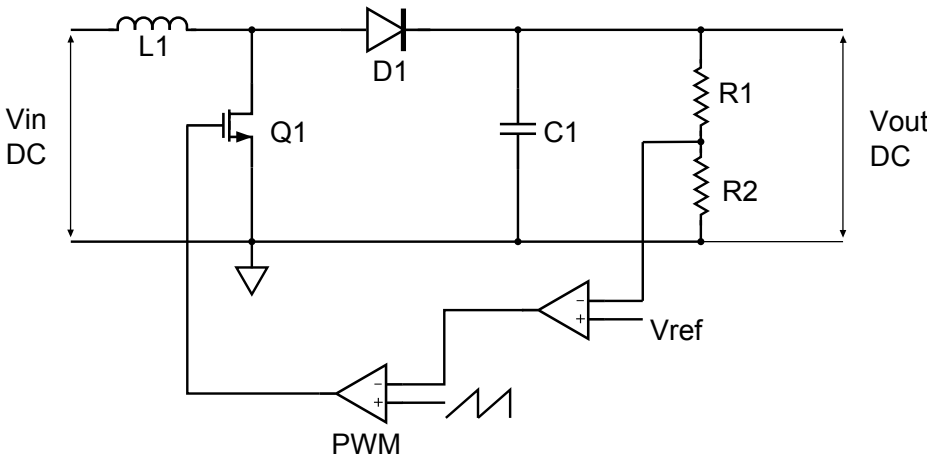


Figure 4.2: Schematic diagram of the boost converter topology.

The boost converter is one of the most frequently used topologies in industrial and consumer applications. Only one switching element is needed, although additional ones can be introduced to increase efficiency. The math behind these converters is well understood and they are easy to design. The necessary coil can easily be obtained from various manufacturers and are offered with different inductances and rated maximum currents. The downside is that boost converters can only output DC current.

Boost converters are able to produce output voltages higher than the input voltage using a magnetic coil for energy storage. It works as follows. When *Q1* is "off", *L1* feeds current to the output capacitator *C1* through the rectifying diode *D1*. If the transistor is turned "on", *D1* is reverse biased and therefore not conducting. Current flows through *L1* and *Q1* to ground. The current through the transistor ramps up linearly to a peak value:

$$I_p = \frac{V_{DC}}{L1} t_{on} \tag{4.1}$$

with t_{on} being the time the transistor is "on". As *D1* is not conducting the load (connected to V_{out}) is supplied only by *D1*. Therefore *C1* has to be large enough to supply the maximum load current for the time t_{on} with a specified minimum drop:

$$C1 = \frac{I_{load}}{V_{ripple}} t_{on}. \tag{4.2}$$

When *Q1* turns off the voltage across the inductor reverses in an attempt to maintain the current constant. The lower end of *L1* goes positive high in respect to the input voltage driving *D1* to forward bias. With *D1* conducting *L1* delivers its stored energy to *C1*. Hence *C1* is brought to a voltage higher than V_{in}. The output voltage is regulated by controlling the time *Q1* is turned "on" in a negative-feedback loop. If load current increases or the input voltage decreases, the "on" period is increased to deliver more energy to the load. If load current decreases or the input voltages increases, the "on" period has to be reduced to keep the output voltage constant.

Losses appear at three points in the basic boost converter circuit: the inductor *L1*, the transistor *Q1* and the diode *D1*. The inductor losses tend to be the most complex to estimate as on top of resistive losses through the windings energy is lost in the stray magnetic field of the coil. In the switching transistor *Q1* mostly resistive losses occur due to its characteristic on resistance. At higher switching frequencies the current necessary to charge and discharge the gate or base capacity can become siginificant and have to be considered eventually. Finally the losses occur in the rectifying diode *D1* as current flows through it. As diodes are p-n-junctions the voltage drop across it determines these losses. Therefore a diode with a low voltage drop is recommended (e.g. Schottky diodes).

As shown in Figure 5.1 the basic boost converter circuit uses only six parts plus the control circuit. That makes it possible to built boost converters occupying little PCB area. The coils used for energy storage are available from several manufacturers in different sizes and with different inductances, therefore meeting even special demands and simplifying the design process. The output voltage of the converter is determined mainly by the control circuit and therefore variable, an important feature in many applications.

Flyback Converter

The flyback converter is similar to the boost converter as in both topologies energy is transported when the switching transistor is turned "off". Therefore the flyback

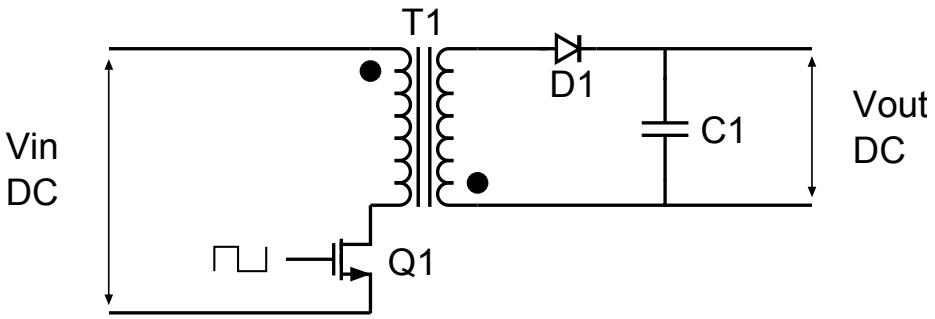


Figure 4.3: Schematic diagram of the flyback converter topology.

transformer works as a choke and therefore has to be designed appliying the rules for inductors. That also is the fundamental difference to the later mentioned transformer based topologies where energy is transferred from primary side to secondary as current flows through both. Looking at the basic schematic for a flyback converter one can see that it is quite similar to a boost converter. The output current is rectified through *D1* and stored in *C1*. The output capacitator *C1* delivers energy to the load when *Q1* is turned "on". The switching transistor *Q1* is driven with a pulse width modulated signal and pulls the primary winding of T1 to ground. The other side of the primary winding is connected to Vin. When *Q1* is "on" current flow through the primary winding of *T1*. The dot ends of both winding are negative in respect of their non dotted ends. *D1* is reverse biased and not conducting. If *Q1* is turned "off" the voltages in the windings immediately reverse. Thus *D1* conducts and current flows to *C1* and the load on the secondary side. As with the boost converter the output capacitator *C1* has to be designed as such to deliver the specified output current at a tolerable voltage drop while *Q1* is "on". The losses in this topology are essentially the same as with boost converters and will not be discussed in greater detail.

As with the boost converter only one switching transistor is needed for basic flyback converter circuit. Only three additional elements are needed for the circuit as shown in Figure 4.3 which simplifies the design and enables compact layouts. However the need for a special flyback "transformer" complicates the component choice as those are less common as for example coils. They are also larger compared to coils.

4.1.2 True DC-AC Inverter Topologies

These topologies are beneficial in that they directly output ac current without further switching elements. The three topologies belonging to this group are the push-pull inverter topology, the full-bridge inverter topology and resonant inverter topologies. The first two are usually employed in DC-DC converter applications but can output

AC current if the rectification at the outputs is omitted. These topologies use transformers and therefore offer galvanic isolation between the low DC input voltage and the high AC output voltage.

Push-pull Converter

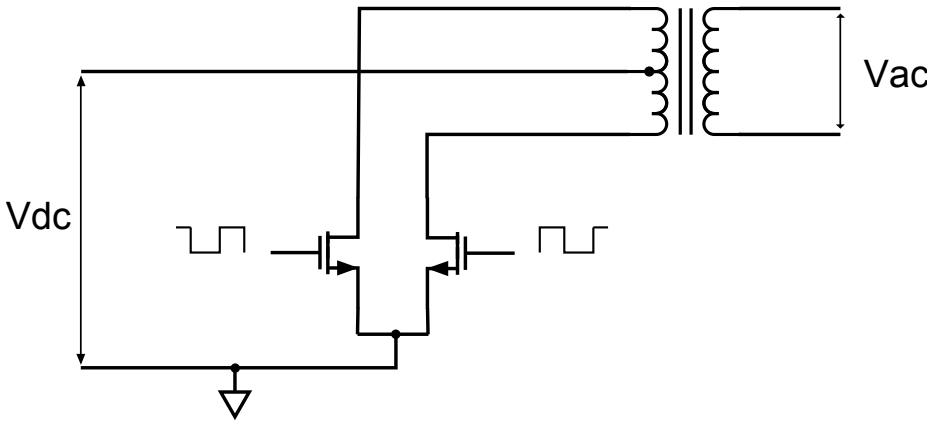


Figure 4.4: Schematic diagram of the push-pull converter topology.

In this topology two transistors drive the two ends of the primary winding alternating to V_{CC} while the center tap is fixed at ground. The result is an ac current with voltage swing of two times V_{CC} seen from the primary winding inducing an AC current in the secondary winding. The turn ratio from primary to secondary side determines the output voltage at the secondary winding:

$$U_2 = \frac{N_2}{N_1} U_1 \tag{4.3}$$

Employing a sinusoidal PWM to drive the primary side transistors and filtering at the output true sinusoidal AC current can be achieved. As the turn ratio is fixed at the construction of the transformer the output voltage can only be varied by the use of PWM. If the output of arbitrary signals and the variation of the output voltage is required, a high resolution PWM is needed. In any case a PWM control circuit is needed to provide the switching waveforms. The general principle behind the PWM control is the same as with boost converters. Losses in this topology occur at two points in the circuit: in the transistors and in the transformer. The transistors mainly cause resistive losses through their given on resistance. these losses can not be avoided entirely but optimized by the choice of transistors with low resistance values. The MOSFETs typically used in this topology also have a characteristic gate

capacity that needs to be charged and discharged by the transistor driving circuit thus causing losses. The transformer also introduces resistive losses through its windings. Although the losses caused by the winding resistance dominates there are also losses caused by imperfections in the magnetic circuit. These are hysteresis losses, eddy currents and magnetostriction.

As Figure 4.4 shows two switching elements and a transformer with center tap is needed for the push-pull topology. These transformers tend to get quite bulky and hard to obtain in low quantities. They are mostly laid out for high power applications and therefore dominate the needed PCB area even when transistors with large cases are used.

H-bridge Converter

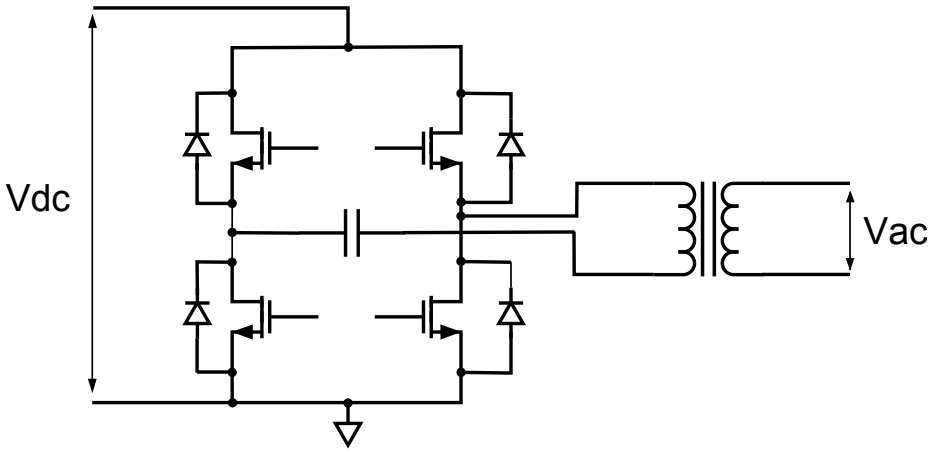


Figure 4.5: Schematic diagram of the H-bridge converter topology.

The H-bridge or full-bridge converter topology is built from four transistors. The transistors can be divided into two pairs of each one transistor connected to the input voltage rail and one conected to ground. These pairs are often referred to as half-bridges and are also used in other applications. Each half-bridge can drive its output to either the input voltage or ground. If the load is connected to two half-bridges the voltage seen from it can effectively be reversed. Therefore the full-bridge arrangement can output a voltage swing double the input voltage. Employing pulse-width modulated signals and a low-pass filter arbitrary waveforms can be generated. To output even higher voltages the H-bridge is connected to a transformer as shown in Figure 4.5. The output voltage is then determined by the input voltage and the winding ratio of the transformer. Power is lost in this topology mainly in the transistors. The power loss therefore tends to get very small if MOSFETs with very

low series resistance are used. If connected to a transformer, magnetic and resistive losses have to be accounted for additionally.

The need for four switching transistors complicates layout and leads to large designs in respect of volume and PCB area. If a transformer is used, the required area increases even further. However, the transformers for this topology tend to be smaller than those in the push-pull converter, as no center tap is needed.

4.2 Resonant Inverter Topologies

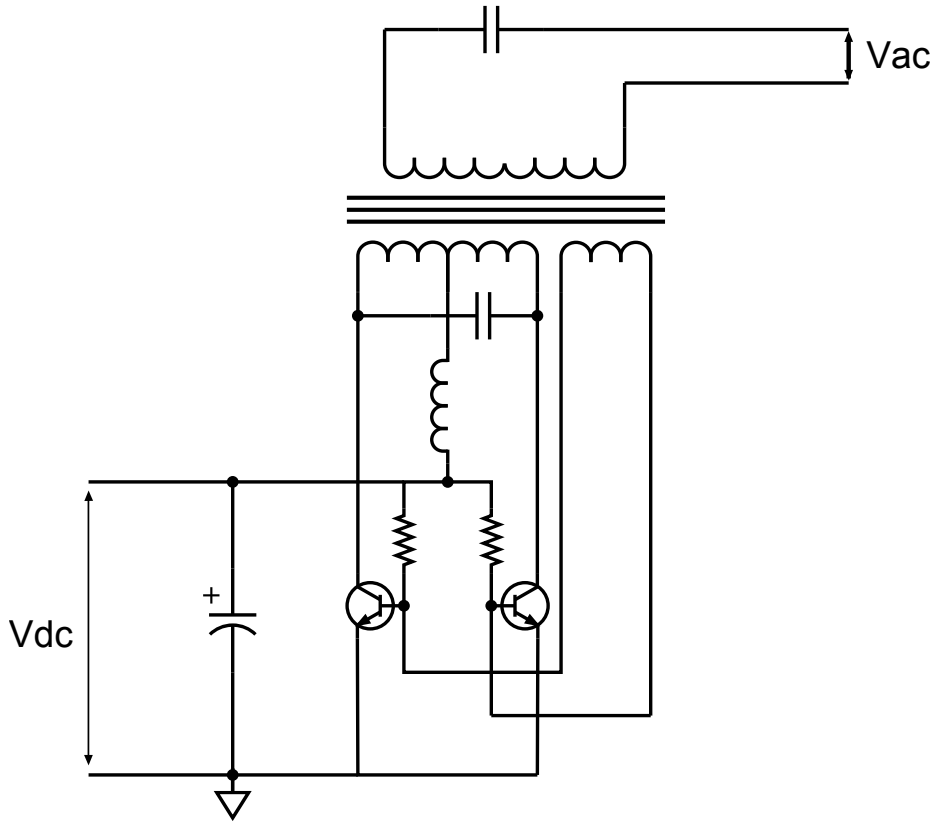


Figure 4.6: Schematic diagram of the Royer converter topology.

Resonant inverter topologies are special in that way that they do not need a control circuit. The feedback directly controls the switching elements. In some resonant topologies the switching element is driven in the linear region which causes high losses even with MOSFETs compared to switchmode topologies. Resonant inverters can be built using SCRs (silicon controlled rectifiers), GTO thyristors (gate turn off

thyristors), MOSFETs or bipolar junction transistors. All resonant inverter topologies employ fairly complex transformers thus making them much harder to design. The complex interaction between the components make these hard to design and even harder to optimize. All resonant topologies output AC current even though only some can provide true sinusoidal voltages. The low component count makes PCB layout easier but the high working frequencies and high currents have to be taken into account. The output voltage and frequency is determined by the component values and are therefore fixed at design time. This makes these topologies less flexible than the aforementioned.

Resonant inverters are difficult to design and properly lay out. The needed parts, foremost the transformer are hard to obtain at least in single quantities. Together with the low efficiency this makes these topologies unsuitable for the planed application and they will therefore not discussed any further.

4.3 Comparison

Topology / Property	**Boost**	**Flyback**
Switching Components	1	1
Type of Magnetic	coil	transformer
Output	DC	DC
Necessary PCB Area	small	small
Output Voltage	variable	variable

(a) DC-DC converter topologies

Topology / Property	**Push-pull**	**H-bridge**	**Resonant**
Switching Components	2	4	2
Type of Magnetic	transformer w/ center tap	none / transformer	transformer
Output	DC / AC	DC / AC	DC / AC
Necessary PCB Area	large	medium	medium
Output Voltage	fixed	fixed	fixed

(b) DC-AC converter topologies

Table 4.1: Comparison of the different topologies.

As Table 4.1 shows each topology has advantages and disadvantages. Since a compact design and configurable output voltage is required in this application the boost-converter topology is the best match. Even though an H-bridge is needed to generate AC output current, the PCB area employed is smaller compared to the other topologies, because no transformer is needed. Since this topology is frequently

used in commercial products, a broad range of controller ICs and matching inductors are available from various distributors. This brings down the part costs even at low volumes for prototyping, which is always an important requirement for university projects. The same applies to H-bridge controllers and high-voltage MOSFETs as these are commonly used in the control of DC motors.

4.4 Conclusion

Several different inverter topologies are compared to each other and finally one of them is chosen. In the end the boost converter fits the requirements at best and is therefore chosen for the implementation. Because the boost converter only outputs DC current, the H-bridge is added to the circuit.

5 Boost converter

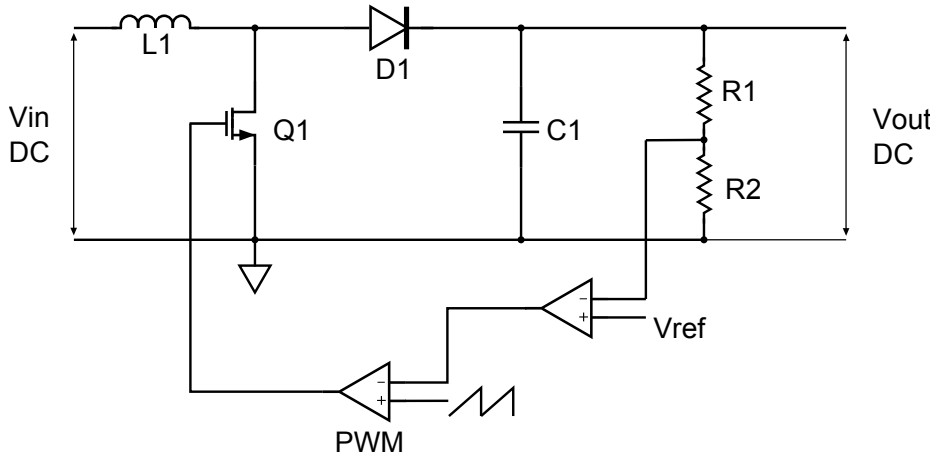


Figure 5.1: Schematic diagram of the boost converter topology.

In the last chapter the boost converter is chosen as the most appropriate topology for the planed application. In order to determine the proper parameters of the parts in boost converter the basic operation and control scheme of this topology will be investigated further. The factors in the circuit which affect the power efficiency will be determined. The final power efficiency of the converter will be calculated. Finally the steps needed to design the boost converter circuit from a set of given requirements will be discussed.

5.1 Basic operation

As mentioned in the last chapter, energy transport from the source to the load only happens, when the switching transistor *Q1* is in the "off" state. When the transistor is turned "on" current only flows through the inductor *L1*. Thus, the boost converter is different from most DC-DC converter topologies. The operation of the boost converter can be divided in two phases, depending on the state of the switch. For the following calculations, steady state conditions and ideal components are assumed.

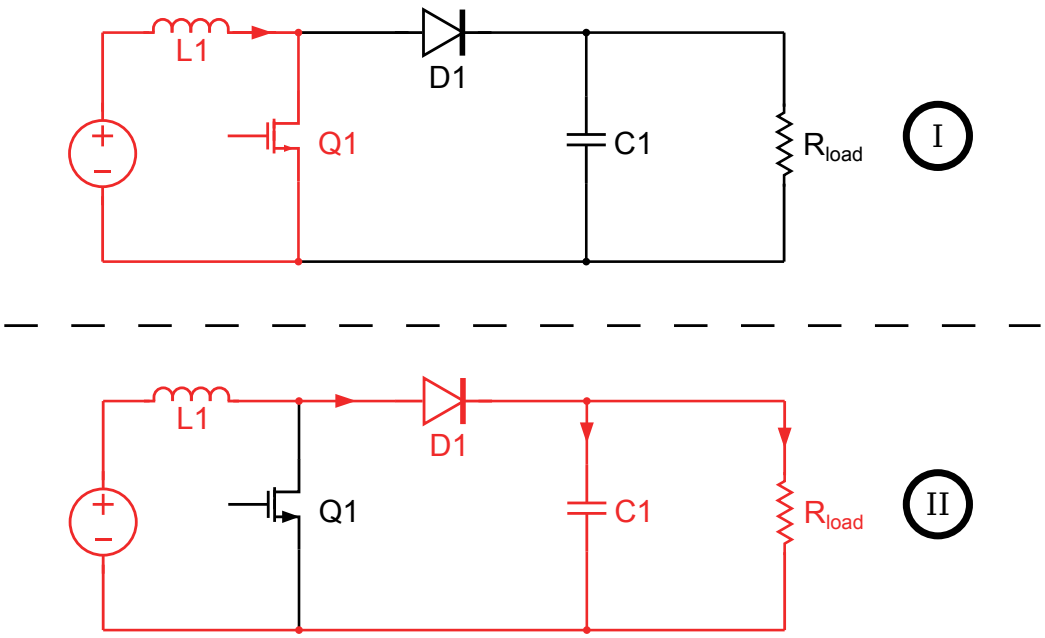


Figure 5.2: The two phases of operation of the boost converter.

Phase I As shown in Figure 5.2 in *Phase I* the current from the voltage source flows through the inductor and the transistor back to ground. As the right side of the conductor is forced to ground, the diode is reverse biased and not conducting. The capacitor *C1* has to deliver current to the load R_{load}. As one side of the inductor is at ground and the other connected to the source, the voltage V_{in} is present across the inductor leading to a change in current through it. The change is given by the following equation:

$$\frac{\Delta I_{L1}}{\Delta t} = \frac{V_{in}}{L1}. \tag{5.1}$$

given that the input voltage V_{in} is constant. At the end of the "on" period the current will have changed by $\Delta I_{L1,on}$, which can be derived from Equation 5.1 by integration:

$$\begin{aligned} \Delta I_{L1,on} &= \frac{1}{L1}\int_0^{T_{on}} V_{in}\mathrm{d}t \\ &= \frac{T_{on}}{L1}V_{in}. \end{aligned} \tag{5.2}$$

T_{on} is the time the switch is in the "on" state. The linear current change is also

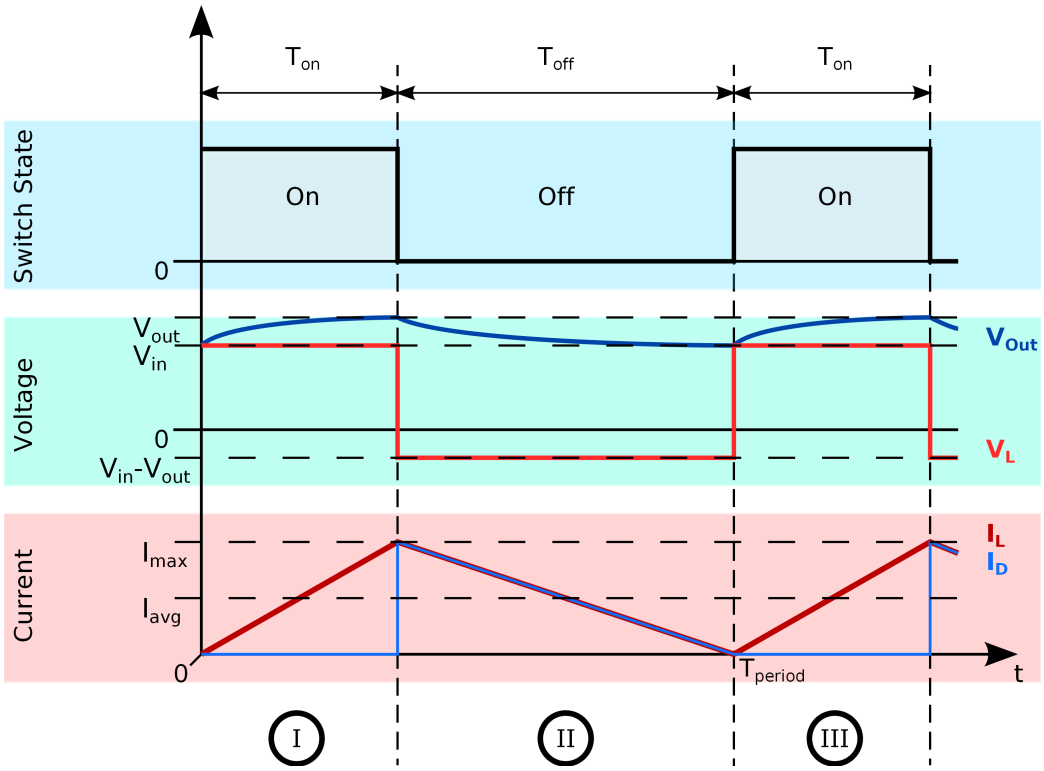


Figure 5.3: Timing diagram of the voltage and current waveforms of the boost converter.

shown in Figure 5.3 as the change from zero current to the maximum current I_{max}. The average current I_{avg} does not change, when the circuit is in a steady state.

Phase II At the end of the "on" period, the transistor is turned "off". The voltage across the inductor *L1* reverses in an attempt to maintain the current flow, which drives the diode *D1* into the forward biased region. Now current flows through the diode to the capacitator *D1* and load resistance R_{load}. The voltage V_{out} on the right side of the inductor is different from the input voltage V_{in}, the current change across it is given by:

$$\frac{\Delta I_{L1}}{\Delta t} = \frac{V_{in} - V_{out}}{L1}. \tag{5.3}$$

The current variation at the end of the "off" period can again be derived from Equation 5.3 by integration:

$$\begin{aligned} \Delta I_{L1,off} &= \frac{1}{L1}\int_0^{T_{off}} (V_{in} - V_{out})\mathrm{d}t \\ &= \frac{T_{off}}{L1}(V_{in} - V_{out}). \end{aligned} \tag{5.4}$$

T_{off} is the time period the switch is turned "off". At the end of the period the current is zero as shown in Figure 5.3. The sum of T_{on} and T_{off} gives the period for one cycle T_{period}.

Phase III This phase is the same as *Phase I*. Diode *D1* is reverse biased again and the load R_{load} is supplied from *C1*. Current flows through *L1* and *Q1* to ground.

When steady state conditions were assumed, the energy energy in the inductor has to be the same at the beginning and end of a period. The energy in an inductor is given by:

$$E = \frac{1}{2}LI_L^2. \tag{5.5}$$

Therefore the total current change over the time T_{period} has to be zero, leading to:

$$\Delta I_{L1,on} = -\Delta I_{L1,off}. \tag{5.6}$$

If $\Delta I_{L1,on}$ and $\Delta I_{L1,off}$ are replaced with the results from Equation 5.2 and Equation 5.4 the following result is reached after rearranging the equation:

$$\frac{V_{out}}{V_{in}} = 1 + \frac{T_{on}}{T_{off}}. \tag{5.7}$$

With the introduction of the duty cycle D that is defined as follows:

$$D = \frac{T_{on}}{T_{on} + T_{off}} \tag{5.8}$$

Equation 5.7 can be written as:

$$D = 1 - \frac{V_{in}}{V_{out}}. \tag{5.9}$$

As Equation 5.9 clearly states that the output voltage of the boost converter solely relies on the duty cycle D, which the transistor *Q1* is driven with. If the transistor is left conducting for a longer time period, the output voltage rises and vice versa.

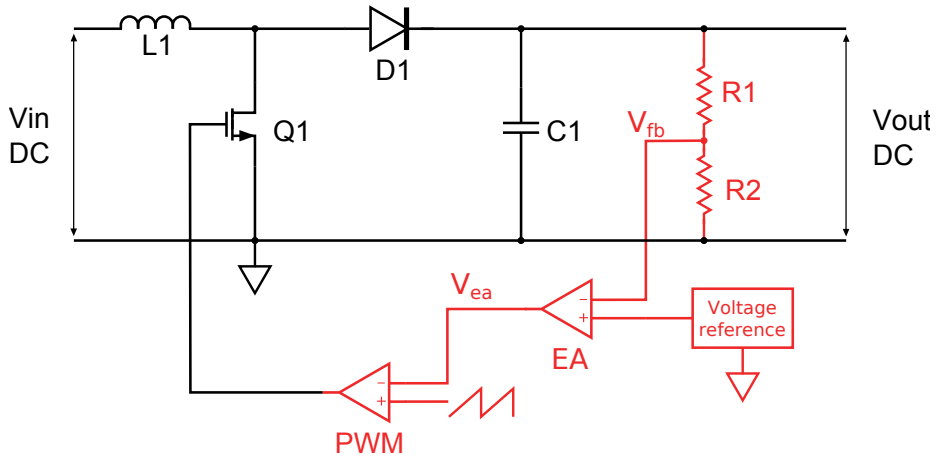


Figure 5.4: Schematic diagram of the boost converter - the control loop is highlighted.

5.2 Control Scheme

It is shown in the last section, that the output voltage of the boost converter is directly proportional to the duty cycle, which the transistor *Q1* is driven with. To ensure a stable output voltage, a closed feedback looped controls the switching transistor with respect to the output voltage. This feedback loop is highlighted in Figure 5.4. It works as follows.

The voltage divider formed by the two resistors *R1* and *R2* sets the output voltage of the boost converter. The voltage V_{fb} is determined by the ratio of the two resistors and the output voltage V_{out}:

$$V_{fb} = \frac{R2}{R1 + R2} V_{out}. \tag{5.10}$$

The error amplifier marked *EA* in Figure 5.4 compares this voltage to a fixed reference voltage and outputs a voltage V_{ea}. If V_{fb} equals the reference voltage it is zero and rises with the difference between these two voltages. Therefore resistances in the voltage divider are chosen such that V_{fb} equals the reference voltage if the desired output voltage V_{out} is reached. The comparator marked *PWM* in Figure 5.4 compared the correcting voltage V_{ea} to a sawtooth shaped waveform and outputs a pulse width modulated signal. If V_{ea} is greater than the sawtooth waveform at a given time, the comparator outputs a high voltage level and thus turns the transistor *Q1* on. If the error voltage V_{ea} is smaller than the current voltage of the sawtooth waveform the output of the comparator is zero. Therefore if the difference between the desired and the actual output voltage increases, the voltage V_{ea} rises and therefore is larger than the sawtooth waveform for a longer time of one period. The duty cycle of the pulse

width modulated signal output by the PWM amplifier increases, thus the output voltage of the converter is increased. In the case of a too large output voltage, the transistor is not turned on at all, as V_{ea} is zero or negative.

This closed feedback loop stabilizes the output voltage of the converter, when the load changes. The capacitor *C1* smoothes the output voltage and acts as energy reservoir, therefore also stabilizes the output voltage.

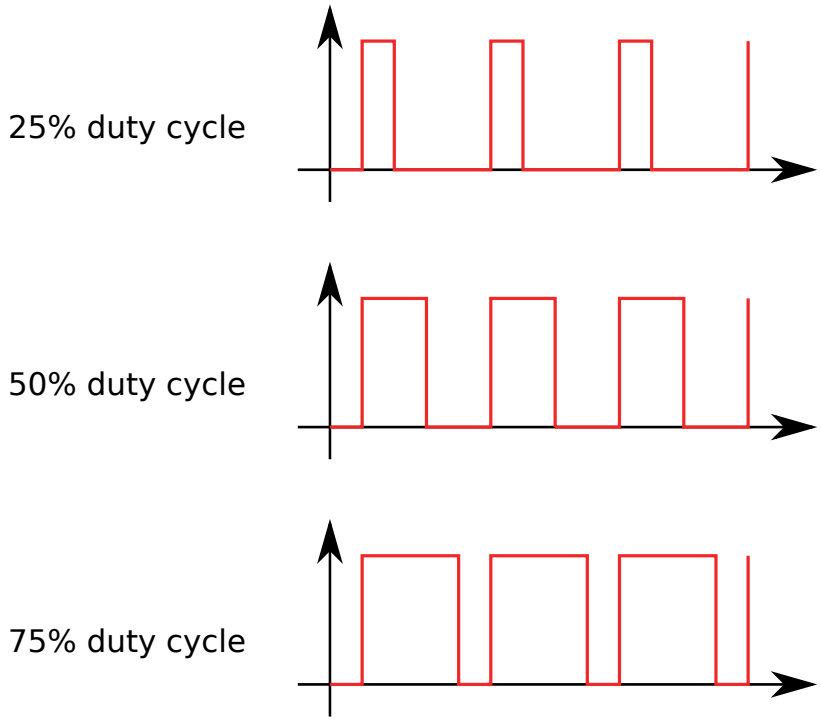


Figure 5.5: Diagram of a pulse width modulated signal at different duty cycles.

Pulse Width Modulation A pulse width modulated signal can be described with two paramaters: its frequency and duty cycle. The frequency is the inverse of the time between the two rising edges of the signal. The duty cycle is the time the pulse is at high or "on" level divided by the time for a period. It ranges between 1 (signal is always high) and 0 (signal is always low). Figure 5.5 shows a pulse width modulated diagram at three different duty cycles.

5.3 Power Efficiency

In Section 5.1 the components in the converter circuit were assumed to be ideal. Components in a real circuit show non-ideal behaviour and first of all introduce energy losses to the circuit reducing its power efficiency. In the following paragraphs the power losses occuring in every single component will be discussed.

Inductor L1 The inductor introduces two types of power losses to the circuit: resistive and magnetic losses. An inductor in its simplest form is a conductor wrapped around a magnetic core. The conductor has a specific electrical resistance that depends mainly on the material it is made of. As current flows through the conductor, the resistance leads to a rise in temperature and an equivalent energy loss. The power loss for a given current can easily be calculated if the series resistance $R_{L1,ser}$ is known:

$$P_{loss,L1} = IR^2. \tag{5.11}$$

The current flow also causes a magnetic field in the inductor. Depending on the actual inductor type hysteresis losses, eddy currents and magnetostriction can lead to energy losses in the magnetic circuit. In most applications the resistive losses dominate and the magnetic losses can be neglected.

Diode D1 A real diode mainly differs from its ideal model in that it has a voltage drop V_F when operated in the forward active region. Although this voltage changes with the current flowing through the diode, it first of all depends of the type of junction used in the device. A typical silicon diode, for example, has a voltage drop of about $V_F = 600\text{mV}$ [19]. The power loss in the diode can be calculated using the following equation.

$$P_{loss,D1} = V_F I \tag{5.12}$$

Capacitor C1 Energy losses in capacitors occur in two ways: stored energy is lost through leakage currents and resistive losses appear in the equivalent series resistance (ESR) of the capacitor as it charges and discharges. The leakage current for electrolytic capacitors usually are between $0.01CV$ and $0.03CV\mu\text{A}$ [19]. When the capacitor is used as power supply reservoir, like in the boost converter circuit the leakage current can be neglected and the losses through ESR have to be accounted for. Two factor determine these losses, the ripple current I_r flowing through the capacitor and its dissipation factor $\tan\delta$. The dissipation factor is expressed as the ratio between the resistive and reactive parts of the impedance [19]:

$$\tan\delta = DF = \frac{ESR}{|X_C|} = \frac{ESR}{\omega C}. \tag{5.13}$$

A value for $\tan\delta$ is usually given in the capacitor's datasheet. For example a Panasonic series EE type A aluminium electrolytic capacitor rated at 200VDC is listed with a value of $\tan\delta = 0.15$ [9]. For a known ripple current I_r, frequency f and capacitance C the power loss can be calculated as follows:

$$P_{loss,C1} = I_r(\tan\delta \cdot 2\Pi f)^2. \tag{5.14}$$

Transistor Q1 Transistors are non-ideal switches and therefore present a resistance to current flowing through them even when driven to saturation. Bipolar junction transistors and MOSFETs are very different in their resistive behaviour. The voltage drop over the bipolar junction transistor (BJT) is nearly constant where the MOSFET appears as a low series resistance. As the losses in modern MOSFET devices tend to be much smaller than those in BJTs, only losses in MOSFETs will be discussed in detail. The series resistance of a MOSFET is typically listed in the datasheet as $R_{DS(ON)}$ and lies in the region of several mΩ for power devices (e.g. $R_{DS(ON)} = 80\text{m}\Omega$ for an International Rectifier IRFB4020PbF [12]). For a given resistance $R_{DS(ON)}$ and current I the power loss can be calculated using Ohm's law:

$$P_{loss,Q1,Rds} = IR_{DS(ON)}. \tag{5.15}$$

This power loss through the series resistance only applies if the transistor is driven to saturation. As the transistor in a boost converter usually is turned "on" and "off" many thousand times per second additional effects have to be considered, too. If the voltage driving the transistor's gate does not rise and fall fast enough, the transistor is in the linear region for the time the voltage is smaller than the threshold voltage. In the linear region the series resistance of the transistor is a function of the gate to source voltage and considerably larger than $R_{DS(ON)}$. For the planed application it is assumed that the turn-on and turn-off time is substantially smaller than one switching period. These power losses can therefore be neglected. The power losses resulting from the charging and discharging of the gate also have to be considered if the device is switched at higher frequencies. The losses can be calculated as follows:

$$P_{loss,Q1,Cgt} = \frac{V_{GS}Q_{gt}}{f_{sw}}. \tag{5.16}$$

In Equation 5.16 symbol V_{GS} denotes the peak of the gate source voltage waveform, Q_{gt} the gate charge and f_{sw} the switching frequency. The total power loss in the transistor is as follows:

$$P_{loss,Q1} = IR_{DS(ON)} + \frac{V_{GS}Q_{gt}}{f_{sw}}. \tag{5.17}$$

Control Circuit and Voltage Divider The supply current of the control circuit and the losses through the voltage divider are negligible: the supply current typically is below 10mA (e.g. $I_{CC} = 4.0$mA for the ON Semi MC34063A [16]) and a current in the region of 100µA through the voltage divider is usually enough to keep the feedback loop stable (e.g. 100µA for a supply voltage from 5to40V for the ON Semi MC34063A [15]).

5.4 Design Process

Table 5.1 shows the equations used to design a boost converter circuit. The equations are taken from the MC34063s datasheet [16] but are essentially the same that have been derived in Section 5.1 and Section 5.2. To design a converter for a certain application, the following parameters have to be extracted from the design requirements:

- the input voltage V_{in},
- the desired output voltage V_{out}
- the maximum output current $I_{out,max}$
- and the maximum output voltage ripple $V_{ripple(pp)}$.

Now the ratio t_{on}/t_{off} can be calculated with the given equation. Given the switching frequency f of the converter (which is limited by the used control circuit) the values for $t_{on} + t_{off}$, t_{off} and t_{on} can be derived.

Now a first constraint for the circuit can be determined, the maximum switch current $I_{pk(switch)}$. The switching transistor in the final circuit has to be chosen accordingly, or if that is not possible, the switching frequency has to be increased. From the maximum switch current, the minimally needed inductance $L_{(min)}$ can be derived. This narrows the choice for a suitable inductor and it might be necessary to change other parameters to adapt the circuit to easily obtainable inductor. One has to pay close attention to the maximum current rating of the inductor as the peak switch current $I_{pk(switch)}$ flows through the inductor, too.

The two parameters left to calculate are the ratio $R1/R2$ of the resistances in the voltage divider and the value for the output capacitor C_O. The ratio of the two feedback resistors can easily calculated for a given V_{in} and V_{out}. The actual resistor values depend on the current through them, that is required to keep the feedback loop stable. A value for this current is typically given in the control circuit's datasheet or application notes. To calculate the value for the output capacitor, the maximum output voltage ripple $V_{ripple(pp)}$ and the average output current I_{out} have to be available. The equation is basically the same as Equation 4.2, however, a safety factor of 9 has been added.

Value	**Calculation**
t_{on}/t_{off}	$\frac{V_{out} + V_F - V_{in}}{V_{in} - V_{sat}}$
$(t_{on} + t_{off})$	$\frac{1}{f}$
t_{off}	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$
t_{on}	$(t_{on} + t_{off}) - t_{off}$
$I_{pk(switch)}$	$2I_{out,max}\left(\frac{t_{on}}{t_{off}} + 1\right)$
$L_{(min)}$	$\left(\frac{V_{in} - V_{sat}}{I_{pk(switch)}}\right) t_{on}$
$R2/R1$	$\frac{V_{out}}{V_{ref}} - 1$
C_O	$9\frac{I_{out} t_{on}}{V_{ripple(pp)}}$

Table 5.1: Equations for the design of a boost converter [16].

After all parameters for the boost converter circuit have been determined, the actual circuit can now be designed and laid out.

6 DC-AC Inverter Design

In the last chapter the operating principle and design equation for the boost converter have been introduced. In this chapter those are used to adapt the topology to the specified application. In addition to the boost converter circuit an H-bridge with according PWM generation is simulated using SPICE software. Based on the simulation results the circuit is optimized for low power consumption in respect to the other aforementioned design parameters.

6.1 Boost Converter

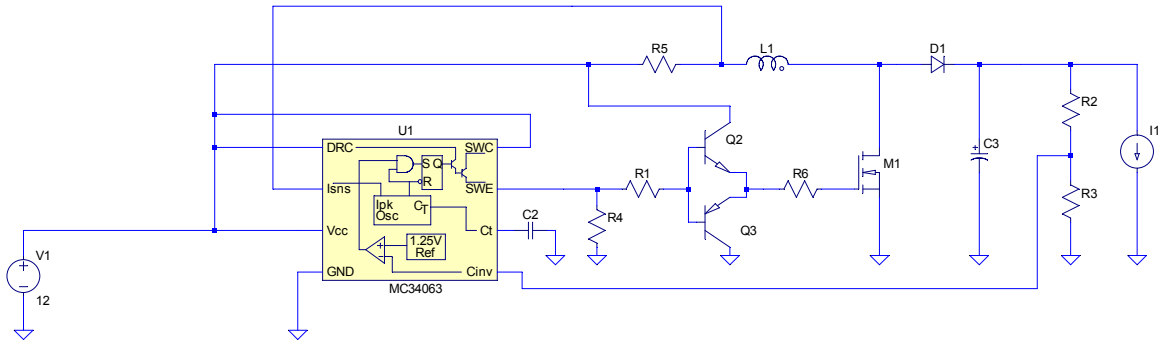


Figure 6.1: Schematic diagram of the boost converter circuit as simulated in LTspice.

The boost converter circuit has been implemented and simulated using the freely available LTspice software from Linear Technology [17]. Figure 6.1 shows the simulated circuit.

6.1.1 Control Circuit

The control scheme as discussed in Section 5.2 had to be implemented in the circuit. As good performance of the control circuit is fundamental for a stable output voltage a reliable solution had to be chosen. The circuit of choice is the MC34063 step-up/down/inverting switching regulator. This versatile device includes all functions

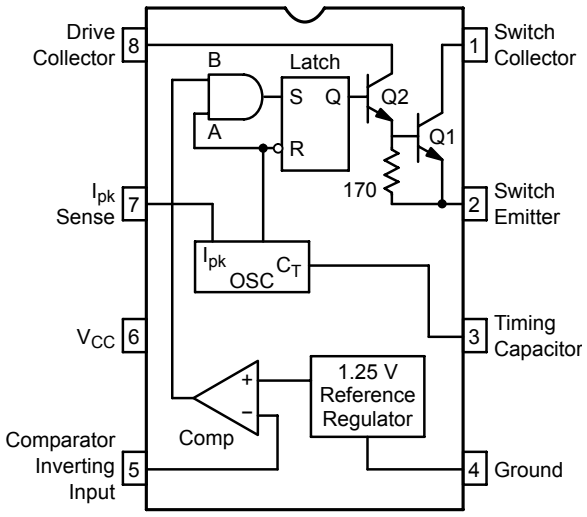


Figure 6.2: Representative schematic diagram of the MC34063 [16].

necessary to build basic DC-DC converter circuits. The device is the successor of the even older μA78S40 and has been around for over 20 years [15]. Even though modern devices offer superior performance over the MC34063 it is still used in countless new designs for its low price, extensive documentation and low requirements to PCB layout. The MC34063 offers a maximum switching frequency of 100kHz [16]. Therefore larger inductance values are needed as with more modern higher frequency devices, but less electromagnetic interference is caused.

In the course of designing the boost converter the results of the design formulas for the MC34063 have to be calculated. At first the parameters for the converter have to be set:

- maximum output voltage of $V_{out} = 60\text{V}$,
- forward voltage drop over the rectifying diode of about $V_F = 1\text{V}$,
- input voltage of $V_{in} = 12\text{V}$,
- voltage drop over the transistor when turned fully on of about $V_{sat} = 1\text{V}$,
- switching frequency of $f = 150\text{kHz}$,
- maximum output current of $I_{out} = 100\text{mA}$,
- peak-to-peak output voltage ripple of $V_{ripple(pp)} = 1\text{V}$.

Most parameters have been taken from the design specifications in Section 2.2. The forward voltage drop is a worst case value and will likely be lower. The voltage drop over the transistor was calculated using the highest value for $R_{DS(ON)}$ from Table 6.2

Value	Calculation	Result
t_{on}/t_{off}	$\frac{V_{out}+V_F-V_{in}}{V_{in}-V_{sat}}$	4.42
$t_{on}+t_{off}$	$\frac{1}{f}$	6.67µs
t_{off}	$\frac{t_{on}+t_{off}}{\frac{t_{on}}{t_{off}}+1}$	1.23µs
t_{on}	$(t_{on}+t_{off})-t_{off}$	5.44µs
C_T	$4.0\cdot 10^{-5}t_{on}$	217pF
$I_{pk(switch)}$	$2I_{out,max}\left(\frac{t_{on}}{t_{off}}+1\right)$	1.08A
R_{SC}	$0.3/I_{pk(switch)}$	0.28Ω
$L_{(min)}$	$\left(\frac{V_{in}-V_{sat}}{I_{pk(switch)}}\right)t_{on}$	55.2µH
$R2/R1$	$\frac{V_{out}}{1.25\text{V}}-1$	48
C_O	$9\frac{I_{out}t_{on}}{V_{ripple(pp)}}$	4.89µF

Table 6.1: Table with design formulas and their results [16].

and a current of 1A. The ripple voltage is not important for this application and therefore chosen fairly large.

Most of the formulas necessary to design the converter were mentioned before in Table 5.1. In Table 6.1 the values for the timing capacitor C_T and the sense resistor R_{SC} have been added.

6.1.2 MOSFET driver

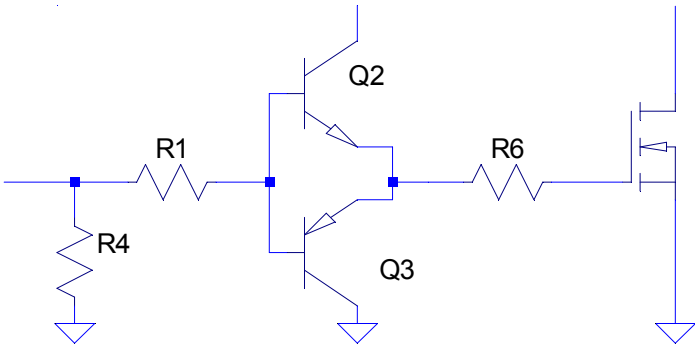


Figure 6.3: Schematic diagram of the MOSFET driver circuit as simulated in LTspice.

The used control circuit only offers an open emitter output and therefore can not drive the gate of a MOSFET directly. An additional driver circuit is necessary to drive the required high voltage, high power MOSFET in the boost converter. The circuit used is illustrated in Figure 6.3. The shown configuration is known under the term totem-pole driver as two transistors sit together back to back. The totem pole configuration is common in countless application from gate drive circuit for high power MOSFETs to outputs in integrated circuits.

For the implementation a configuration consisting of two bipolar junction transistors were chosen, as these were easy to interface to the open emitter output of the control circuit [19]. The circuit works as follows. When the output of the control circuit is turned “on” the voltage at the emitter equals V_{CC} minus one diode drop. The base voltage of the upper NPN transistor is higher than its emitter voltage and current flows from its emitter to the collector in effect charging the gate of the MOSFET. When the gate voltage of the MOSFET exceed its threshold voltage it too starts conducting. The output of the control circuit is then turned “off”. The lower PNP connector is connected to ground via the two base resistors. As the gate of the MOSFET is still charged the lower transistor starts conducting till the gate voltage is zero plus one diode drop. The gate voltage is smaller than the threshold voltage and no more current flows through the MOSFET.

For the bipolar junction transistors a pair of complimentary types was chosen to ensure symmetry for the charging and discharging of the gate capacitance.

6.1.3 MOSFET Selection

For the selection of the most suitable n-channel MOSFET a list with devices matching the requirements was made. Table 6.2 shows the devices that went into the simulation and were compared to each other in terms of lowest possible power consumption. The criteria for the selection were as follows:

- maximum drain to source voltage V_{DS} of at least 100V,
- maximum continous drain current I_D of at least 1A,
- an easy to handle case (e.g. TO220-AB),
- an as low as possible gate charge Q_{gt},
- a price below 5 EUR for single quantities and
- availability through a distributor (e.g. Farnell).

6.1.4 Diode Selection

For the selection of the best matched diode a list of suitable devices was made again. The devices that went into simulation are shown in Table 6.3 with their most important characteristics. The requirements for the diodes were as follows:

- maximum forward current of at least $I_O = 1\text{A}$,
- peak reverse voltage of at least $V_R = 100\text{V}$,
- as small as possible reverse recovery time t_{rr},
- as low as possible forward voltage drop V_{FM}.

6.1.5 Simulation

As was mentioned before the simulation is done in LTspice. For the resistors, capacitors, inductances, voltage and current sources and bipolar junction transistors, models supplied with the software were used. In addition several third party SPICE models were used: a MC34063 model made by intusoft and several diode and MOSFET models supplied from the respective manufacturers.

Manufacturer	Part No.	max. V_{DS}/V	max. I_D/A	max. $R_{DS(ON)}/\Omega$	max. Q_{gt}/nC	Case
IR	IRF740	400	10.00	0.550 @10V 5.2A	63.0	TO-220AB
IR	IRFB4227PbF	200	65.00	0.024 @10V 46A	98.0	TO-220AB
IR	IRFI4227PbF	200	26.00	0.025 @10V 17A	110.0	TO-220AB
IR	IRFB4620PbF	200	25.00	0.072 @10V 15A	38.0	TO-220AB
IR	IRFB4020PbF	200	18.00	0.100 @10V 11A	29.0	TO-220AB
IR	IRFR220N	200	5.00	0.600 @10V 2.9A	23.0	D-PAK
IR	IRF620PbF	200	5.20	0.800 @10V 3.1A	14.0	TO-220AB
IR	IRF624PbF	250	4.40	1.100 @10V 2.8A	14.0	TO-220AB
STM	STF19NF20	200	15.00	0.160 @10V 7.5A	24.0	TO-220AB

Table 6.2: Comparison of suitable n-channel MOSFETs for the boost converter.

Manufacturer	Part No.	max. V_{RRM}/V	max. I_O/A	max. t_{rr}/ns	max. V_{FM}/V
Diodes Inc.	ES2B	100	2	25	0.92
Diodes Inc.	ES2C	150	2	25	0.92
Diodes Inc.	ES2D	200	2	25	0.92
Diodes Inc.	ES3B	100	3	25	0.90
Diodes Inc.	ES3C	150	3	25	0.90
Diodes Inc.	ES3D	200	3	25	0.90
Diodes Inc.	MURS320	200	3	25	0.90
Diodes Inc.	UF3003	200	3	50	1.00
Diodes Inc.	PDU420	200	4	25	0.89
Diodes Inc.	RS3B	100	3	150	1.30

Table 6.3: Comparison of suitable ultra-fast rectifier diodes for the boost converter.

6.1.6 Optimization

The optimization has been split up in several parts each optimizing one core component of the boost converter. For simple components like the inductor and the resistors the value was sweeped and the power efficiency calculated for each one. The value with the highest efficiency was chosen. For complex components like the bipolar junction transistors, the MOSFET and the diode models for several different devices were substituted and the efficiency calculated for each. The one with the highest efficiency was again chosen.

Inductor

L1	**Power Efficiency η**	**Average Output Voltage $V_{out(avg)}$**
22µH	75.39%	53.77V
47µH	81.98%	55.54V
68µH	80.98%	58.14V
100µH	80.40%	59.95V
150µH	79.64%	59.85V
180µH	79.77%	59.82V
220µH	80.04%	59.80V
470µH	79.07%	59.49V
680µH	83.93%	59.36V

Table 6.4: Results from the simulation with different inductance values for *L1*.

The inductance value was not swept over an continuous interval, rather distinct values were chosen and simulated. These values were taken from the E-series as inductors are usually manufactured and sold with these values. In addition to the systems power efficiency the average output voltage was calculated. The value that was finally chosen is $L1 = 100\mu H$, as it is the efficiency peak under the constraint of maximum output voltage.

MOSFET Driver

Two different complementary transistor pairs were simulated for the MOSFET driver: BC547C, BC557C and BC807-40, BC817-40. The difference in efficiency between those was insignificant in the simulation. The BC807-40 and BC817-40 were ultimately chosen for their smaller size (surface mount package SOT-23).

Gate Resistor

The circuit was simulated without a gate resistor and with $R_{gt} = 24\Omega$. The power efficiency was the same for both. Therefore a gate resistor of 24Ω was chosen to limit the current through the gate driver transistor to their respective maximum current (500mA).

Base Resistor

The base resistor of the transistor pair driving the MOSFET gate has to be chosen small enough to allow enough base current to saturate both transistors. This guarantees the highest possible switching speed. The current gain of the BC807-40 and BC817-40 bipolar junction transistor is $h_{FE} = 40$ minimum [6, 7]. For a voltage $V_{CC} = 12V$ and collector current $I_C = 500mA$ the maximum base resistance can be calculated:

$$R_{base} \leq V_{CC} \frac{h_{FE}}{I_C} = 960\Omega. \tag{6.1}$$

Again, the value for the two base resistors *R3* and *R4* was not swept over a continous interval. Instead several distinct values were taken from the E24-series. The highest efficiency was calculated for a value of $R_{base} = 620\Omega$.

Diode

As for the rectifying diode *D1* the simulation was done with ten different devices. The SPICE models for the devices were supplied from the manufacturer Diodes Inc. The

diodes used in the simulation are listed in Table 6.3 with the corresponding power efficiency.

D1	**Power Efficiency η**
ES2B	79.92%
ES2C	79.92%
ES2D	79.92%
ES3B	79.92%
ES3C	79.92%
ES3D	79.92%
MURS320	80.01%
UF3003	78.30%
PDU420	80.12%
RS3B	74.60%

Table 6.5: Results from the simulation with different diodes for *D1*.

Even though the part No. PDU420 offered the highest power efficiency, the second best device, Part No. MURS320 was chosen. The reason herefore lies in the unavailability of the Part No. PDU420 through the distributor at the time of writing.

MOSFET

For the MOSFETs listed in Table 6.2 SPICE simulation models were downloaded from the website of the respective manufacturer and included in the boost converter circuit. The power efficiency of the whole circuit was measured for each of these devices. The results can be found in Table 6.6.

The International Rectifier IRFB4020PbF offered the highest efficiency with 84.20% and was therefore chosen for the implemenation.

Conclusion

After the whole circuit has undergone optimization it reaches a power efficiency of over 84% in the simulation. This is a very good result, bearing in mind that an efficiency of $\geq 90\%$ is considered high effiency for modern DC-DC converters and the used control circuit MC34063 is over 20 years old.

M1	Power Efficiency η
IRF740	82.52%
IRFB4227PbF	83.04%
IRFI4227PbF	83.04%
IRFB4620PbF	83.87%
IRFB4020PbF	84.20%
IRFR220N	83.09%
STF19NF20	80.76%
IRF620PbF	82.85%
IRF624PbF	82.85%

Table 6.6: Results from the simulation with different MOSFETs for *M1*.

6.2 H-bridge

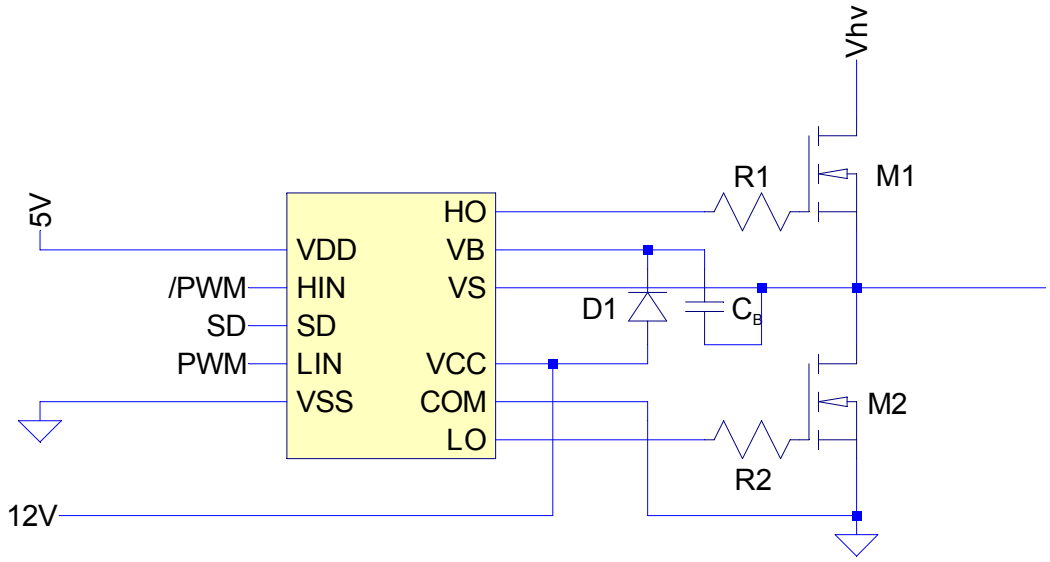


Figure 6.4: Schematic diagram of one half-bridge as simulated in LTspice.

The H-bridge is connected to the high voltage output of the boost converter to generate the required AC current. By turning either half-bridge "on" or "off" the voltage at the output can effectively be reversed thus creating an AC waveform. In order to improve the power efficiency of the H-bridge it was decided to use n-channel MOSFETs for the high- and low-side of each half-bridge. The reason herefore lies in the lower on resistance of n-channel MOSFETs compared to their p-channel counterparts [5]. The problem that arises when a n-channel device is used for high-

side switching is the required gate voltage. The gate voltage has to be $10 - 15V$ higher than the source voltage to turn the device fully "on". In a high-side switching application the drain is connected to the voltage that is to be switched and usually this is the highest voltage in the system. The voltage drop over the transistor is usually very low as a transistor with a low on-resistance is used. The source voltage is close to the drain voltage, thus making it impossible to switch the transistor with the given drain voltage. This applies to the given circuit. Therefore an additional voltage is needed that is higher than the drain voltage. It has to be generated by the driver circuit.

6.2.1 Driver Circuit

For the implementation a gate driver circuit integrating most functions required to drive a half-bridge with two n-channel MOSFETs was chosen. The integrated circuit chosen is the IR2110 manufactured by International Rectifier. Because of its low price, high availability and extensive documentation the IR2110 is a good match for this application. It also meets the voltage and switching speed requirements mentioned before. Last but not least it is available in easy to use packages like PDIP (Plastic Dual-Inline Package) and SOIC (Small Outline Integrated Circuit) that can be handled without special equipment.

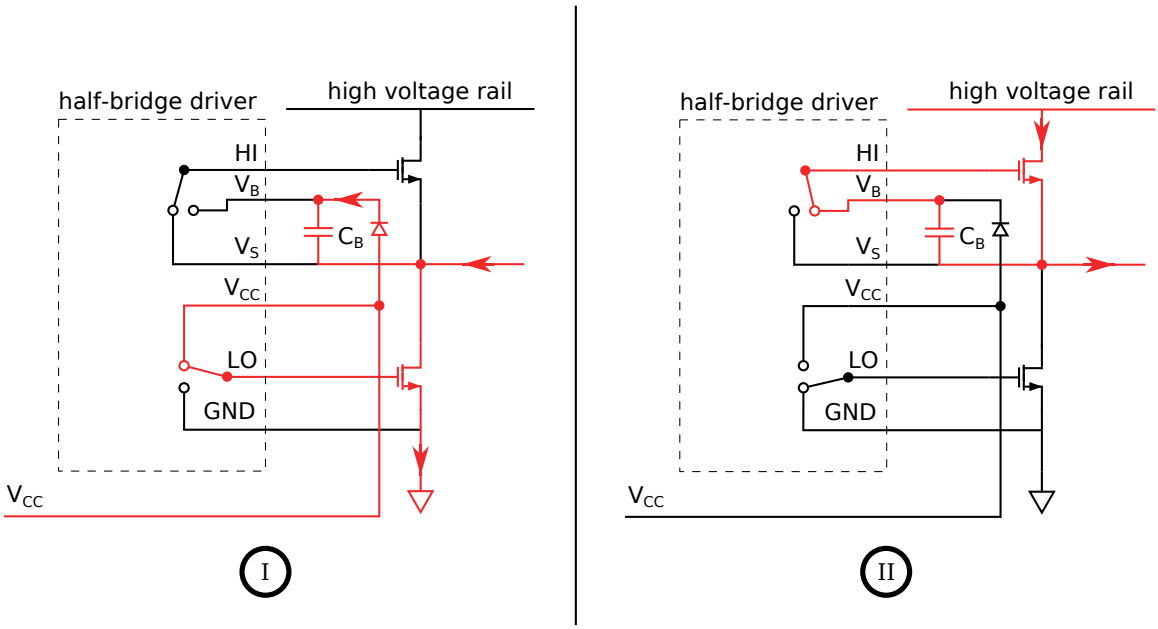


Figure 6.5: Diagram of the bootstrap operation.

To generate the needed gate drive voltage for the high-side MOSFET the IR2110 is

designed for so called bootstrap operation [11]. The bootstrap circuit works as follows. In *Phase I* the low-side FET is turned "on" by the driver circuit by pulling its gate to V_{CC}, which is above its threshold voltage. The high-side FET is not conducting as its gate is at the same voltage as its source. The diode is forward biased and the bootstrap capacitor C_B is charged with the voltage V_{CC}. Now gate of the low-side FET is connected to ground and stops conducting. That leads to *Phase II*. Now the gate of the high-side FET is connected to the upper end of the bootstrap capacitor C_B. The gate voltage is now higher than the source voltage by V_{CC}, thus the transistor starts conducting. The gate capacitance of the transistor is very small thus the voltage at the capacitor and the gate stays the same. The voltage at the the output is rising to the voltage of the high voltage rail. Even though the lower side of the capacitor is charged the voltage difference over it stays at V_{CC}. Therefore the high-side transistor keeps conducting until its gate is disconnected from the bootstrap capacitor and forced to the level of its source connection.

For the operation of the IR2110 at least two additional components are needed: the diode *D1* and the bootstrap capacitor C_B (see Figure 6.4). The diode has to meet the following requirements:

- reverse blocking voltage of $V_{hv} = 60\text{V}$,
- current rating of $I_O \geq 20\text{kHz} \cdot 29\text{nC} = 0.6\text{mA}$,
- ultra-fast rectifier diode [13].

The diodes that were used in the simulation will be discussed later. To calculate the needed bootstrap capacitor C_B a design formula from an International Rectifier Application Note was used [13]. The circuit parameters have to be determined before the calculation can be done:

- gate charge of the upper MOSFET $Q_g = 29\text{nC}$ [12],
- operation frequency $f = 20\text{kHz}$,
- bootstrap capacitor leakage current $I_{Cbs(leak)} \approx 0\text{A}$ [13],
- maximum V_{BS} quiet current $I_{qbs(max)} = 230\mu\text{A}$ [11],
- logic section voltage source $V_{CC} = 12\text{V}$,
- forward voltage drop across the bootstrap diode $V_f \approx 1\text{V}$,
- voltage drop across the low-side FET or load $V_{LS} \approx 0\text{V}$,
- minimum voltage between V_B and V_S $V_{Min} = 10\text{V}$ [12],
- level shift charge required per cycle $Q_{ls} = 5\text{nC}$ [13].

Using these parameters the value for the boostrap capacitor can be calculated:

$$C_{B(min)} = \frac{2\left[2Q_g + \frac{I_{qbs(max)}}{f} + Q_{ls} + \frac{I_{Cbs(leak)}}{f}\right]}{V_{CC} - V_f - V_{LS} - V_{Min}} = 135\text{nF}. \tag{6.2}$$

6.2.2 Part Selection

The MOSFETs listed in Table 6.7 have been used in the simulation of the H-bridge circuit. Most of the devices have already been used in the simulation of the boost converter, as both circuits have the same drain-to-source voltage requirements and profit from a low as possible gate charge. Two devices were added that did not fulfill the drain current requirement of the boost converter but can be used for the H-bridge. As the devices in Table 6.2 have been chosen according to these criteria they were carried over to this circuit. The same applies to the diode in the bootstrap diode. The devices listed in Table 6.3 were therefore used again.

6.2.3 Simulation

One half-bridge built around the IR2110 is shown in Figure 6.4. For the simulation two half-bridge circuits were combined to an H-bridge and connected to a resistive load. The load was chosen to be greater than the measured values of the EL panel implied, so to calculate for the worst case. The control signal *PWM*, */PWM* and *SD* were generated with voltage sources in pulse-mode and included a dead-time between the edges of *PWM* and */PWM*.

6.2.4 Optimization

Diode

The simulation was undergone with the ten devices listed in Table 6.3. As the results for the parts ES2B, ES2C, ES2D and ES3B, ES3C, ES3D were the same only one member of the two lines of rectifying diodes was included in the results. The simulation results are shown in Table 6.8.

Even though the part no. ES3D offered the highest power efficiency of all, the MURS320 is chosen for its lower price and similar performace. As it is already used in the boost converter circuit the cost for the whole circuit can be reduced further by economies of scale.

Manufacturer	Part No.	max. V_{DS}/V	max. I_D/A	max. $R_{DS(ON)}/\Omega$	max. Q_{gt}/nC	Case
IR	IRF740	400	10.00	0.550 @10V 5.2A	63.0	TO-220AB
IR	IRFB4227PbF	200	65.00	0.024 @10V 46A	98.0	TO-220AB
IR	IRFI4227PbF	200	26.00	0.025 @10V 17A	110.0	TO-220AB
IR	IRFB4620PbF	200	25.00	0.072 @10V 15A	38.0	TO-220AB
IR	IRFB4020PbF	200	18.00	0.100 @10V 11A	29.0	TO-220AB
IR	IRF5801	200	0.60	2.200 @10V 0.36A	3.9	TSOP-6
IR	IRFR220N	200	5.00	0.600 @10V 2.9A	23.0	D-PAK
IR	IRF7464	200	1.20	0.730 @10V 0.72A	14.0	SO-8
IR	IRF620PbF	200	5.20	0.800 @10V 3.1A	14.0	TO-220AB
IR	IRF624PbF	250	4.40	1.100 @10V 2.8A	14.0	TO-220AB
STM	STF19NF20	200	15.00	0.160 @10V 7.5A	24.0	TO-220AB

Table 6.7: Comparison of suitable n-channel MOSFETs for the H-bridge.

D1	Power Efficiency η
ES2D	99.54%
ES3D	99.66%
MURS320	99.57%
UF3003	99.15%
PDU420	99.48%
RS3B	99.48%

Table 6.8: Results from the simulation with different diodes for *D1*.

MOSFET

For each MOSFET in Table 6.7 the simulation was done and the power efficiency calculated. The results are shown in Table 6.9.

M1	Power Efficiency η
IRF740	99.32%
IRFB4227PbF	99.18%
IRFI4227PbF	99.18%
IRFB4620PbF	99.58%
IRFB4020PbF	99.66%
IRF5801	98.57%
IRFR220N	99.41%
IRF7464	99.51%
STF19NF20	99.45%
IRF620PbF	99.37%
IRF624PbF	99.22%

Table 6.9: Results from the simulation with different MOSFETs for *M1* and *M2*.

Again the IRFB4020PbF made by International Rectifier was chosen. It offered the highest power efficiency of the devices.

Conclusion

After the choices for the diode and MOSFET were optimized the H-bridge circuit offers an overall efficiency of over 99%. This is no suprising result, as H-bridges usually are very efficient under the premise of MOSFETs with very low series resistances. It is very likely that the implemented circuit offers a similar performance.

6.3 PWM Generation

In contradistinction to the control circuit used in the boost converter the driver circuit for the H-bridge needs control signals. To be able to change the output frequency and to dim the EL lamp a circuit with freely programmable PWM generation is required. There are several different approaches to this problem: distinct logic chips and timers, programmable logic (FPGAs, CPLDs), discreet transistor logic and a microcontroller. Ultimately the microcontroller was chosen, as this solution is the most flexible and has the lowest part count. The possibility to add an easy to use user interface to change the PWM parameters (frequency, duty cycle) to the circuit is beneficial, too.

6.3.1 Microcontroller

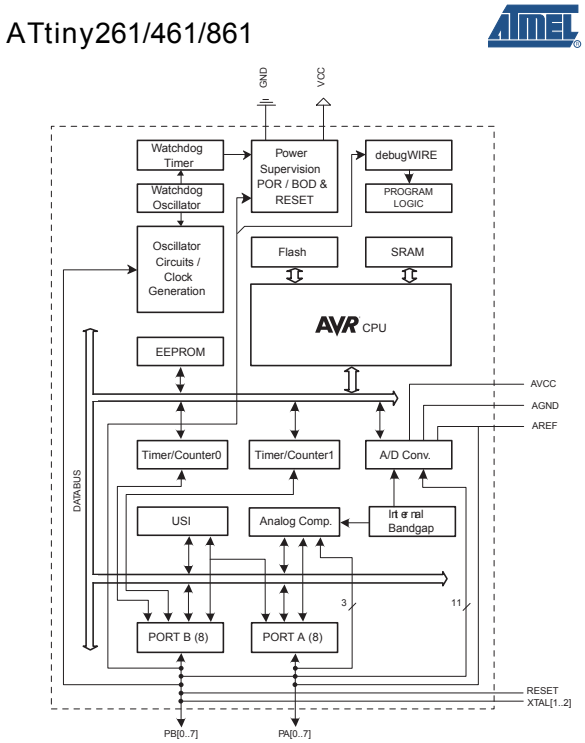


Figure 6.6: Block diagram of the Atmel ATtiny261 8-bit microcontroller [2].

The microcontroller chosen for this task is the ATtiny861 from Atmel. It offers an 8-bit CPU core, 8KB in-system-programmable program memory flash, 512B internal SRAM and 512B in-system-programmable EEPROM. The system clock can be run up to 20MHz, thus offering comparably high computing power in a small package. The most outstanding feature of the ATtiny861 are its advanced PWM generation

capabilities, providing three PWM channels with seperate output compare registers and programmable dead time generator. For the application at hand only two PWM channels are needed. The integrated PWM facilities made it possible to develop the control program in a short time.

A block diagram of the ATtiny861 is shown in Figure 6.6. The PWM generation functions are integrated with *Timer/Counter1* and connected to the I/O port *PORT B*.

6.3.2 Control Program

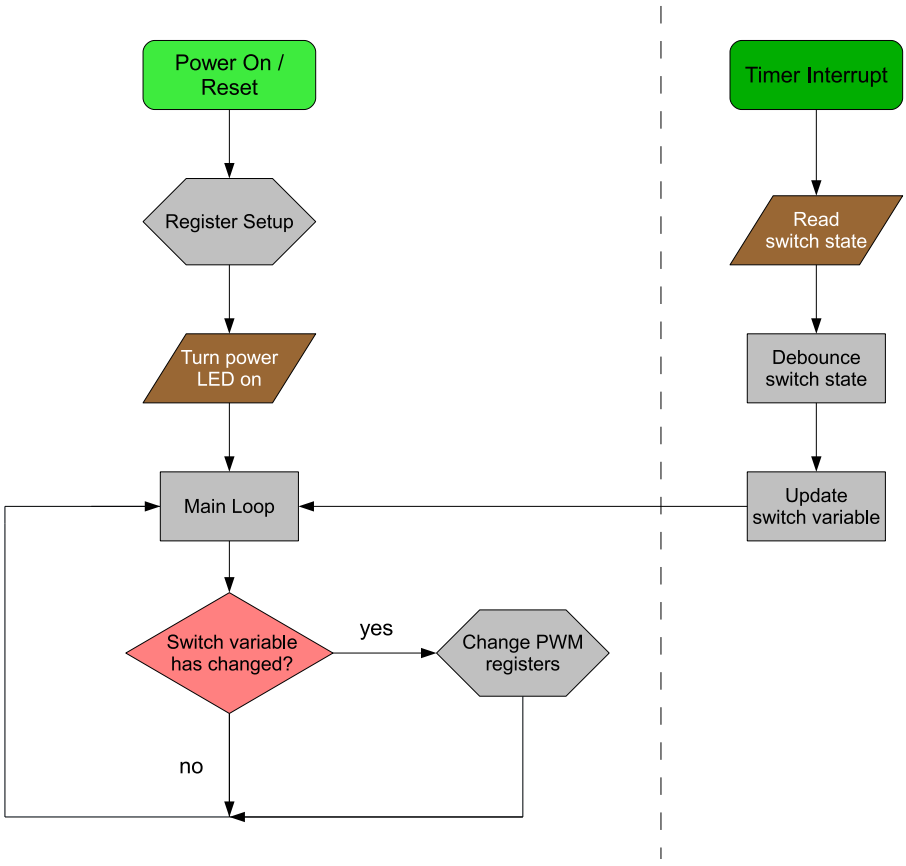


Figure 6.7: Flow chart diagram of the control program.

The control program that was loaded in the program flash of the ATtiny861 microcontroller consists of three main parts: the register setup, the main loop and an

interrupt routine. A flow chart diagram of the program is shown in Figure 6.7. The full C source code can be found in the Appendix.

When the controller is powered up or reset the register setup is executed. It sets the required registers for the I/O ports, the *Timer0* used for interrupt generation and the *Timer1* controlling the PWM signals. After the setup the processor enters the main loop. This loop is executed indefinitely. It checks the switch state variable for changes and if so, updates the PWM registers accordingly. The interrupt routine operates in parallel to the main loop and is executed every 10ms. It reads the I/O pins to which the switches are connected for changes. As all mechanic switches bounce when turned [19], the input level transitions caused by this have to be filtered out. This is also done in the interrupt routine. The debounced switch state is saved in a global variable that is read in the main loop.

6.4 Simulation

After both circuits have been optimized they were combined in one schematic to simulate and calculate the performance of the whole system. As it was not possible to include a microcontroller in the simulation, the PWM control signals have been modeled with voltage sources. The datasheet did not contain a value for the power consumption of the microcontroller under the given conditions [2]. Therefore the highest listed value was taken (I_{CC} = 9mA). The circuit was simulated with a switching frequency of f = 4000Hz and an output voltage of V_{HV} = 60V. Figure 6.9 shows the resulting output waveform. The output of the H-bridge is connected to the electrical equivalent model of the EL panel. The values for the components were taken from Table 3.1. The schematic diagram as entered in LTspice is shown in Figure 6.8.

After the simulation finished, the circuit's power efficiency was calculated using the integrated features of LTspice. The resulting power efficiency is η = 88.53%. The power efficiency for the complete circuit is higher than the one for the boost converter mentioned in Section 6.1, because the load presented by the EL panel's equivalent circuit is much lower than that in the simulation of the boost converter.

6.5 Evaluation

No actual data on the power efficiency of commercially available EL panel inverters could be found. This could be due to the nature of EL panels, because the load from different panels can vary tremendously. However, data on the power efficiency of several different DC-DC converter circuits was extracted from the manufacturers

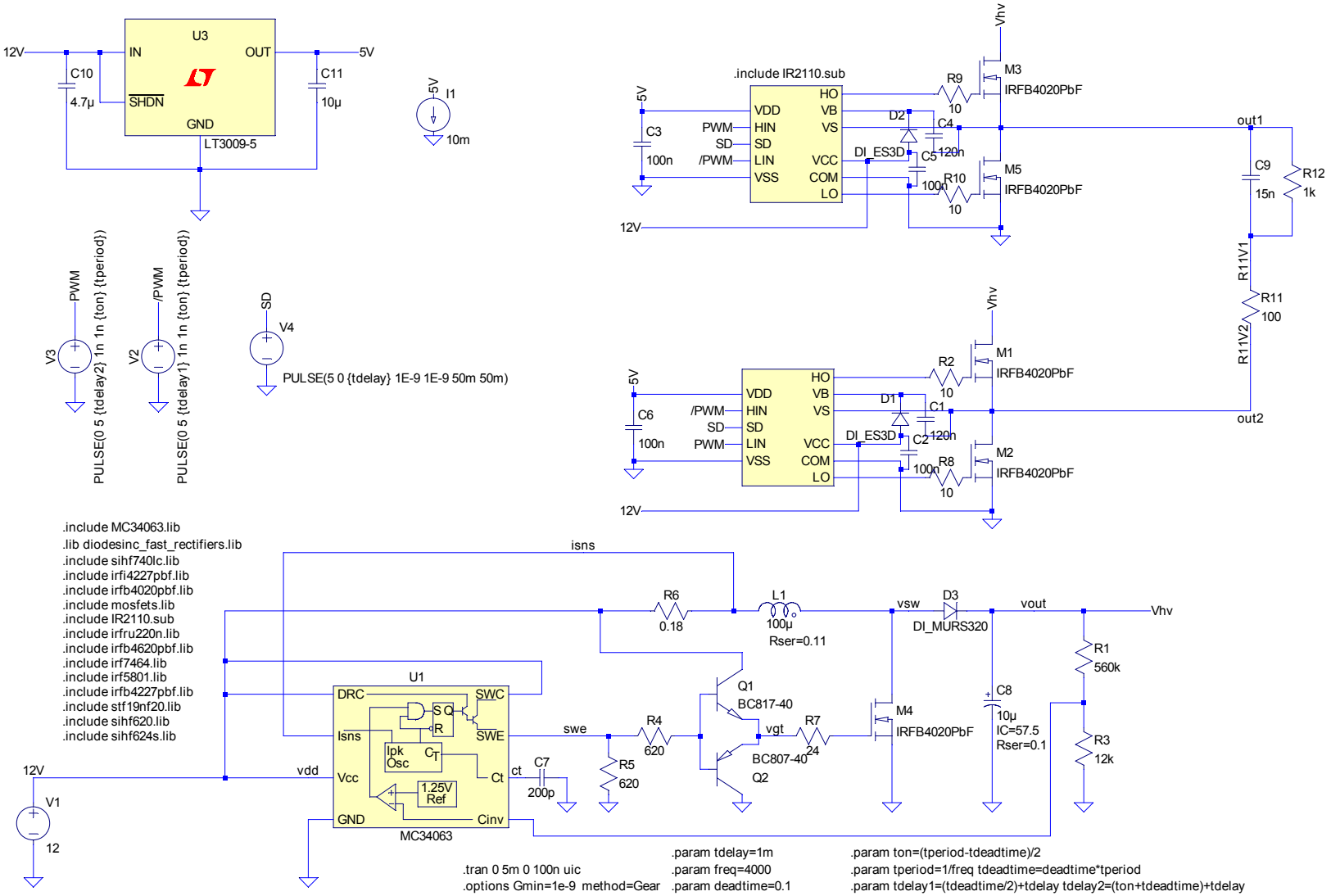


Figure 6.8: Schematic diagram of the DC-AC inverter circuit as simulated in LTspice.

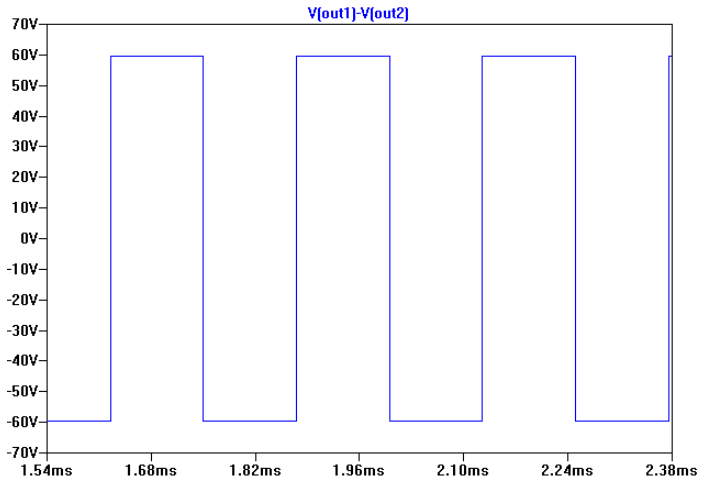


Figure 6.9: Output waveform of the simulated DC-AC inverter circuit.

This Work	88.42%	@ $V_{OUT} = 60\text{V}$, $I_{OUT} = 150\text{mA}$
Texas Instruments TPS61085	90%	@ $f = 650\text{kHz}$, $L = 6.8\mu\text{H}$, $I = 150\text{mA}$, $V_{in} = 3.3\text{V}$, $V_S = 12\text{V}$
Texas Instruments TPS40210	$\sim 90\%$	@ $I_{LOAD} \approx 150\text{mA}$, $V_{IN} = 8\text{V}$
aimtec AM2F-0524SZ	68%	@ $V_{IN} = 5\text{V}$, $V_{OUT} = 24\text{V}$, $I_{OUT} = 83\text{mA}$

Table 6.10: Comparison of the efficiency of the designed boost converter to other existing designs.

datasheets and is shown in Table 6.10. The results for the designed circuit is a bit lower than those for the more current Texas Instruments devices, but higher than those for the integrated DC-DC converter module from aimtec.

7 Implementation

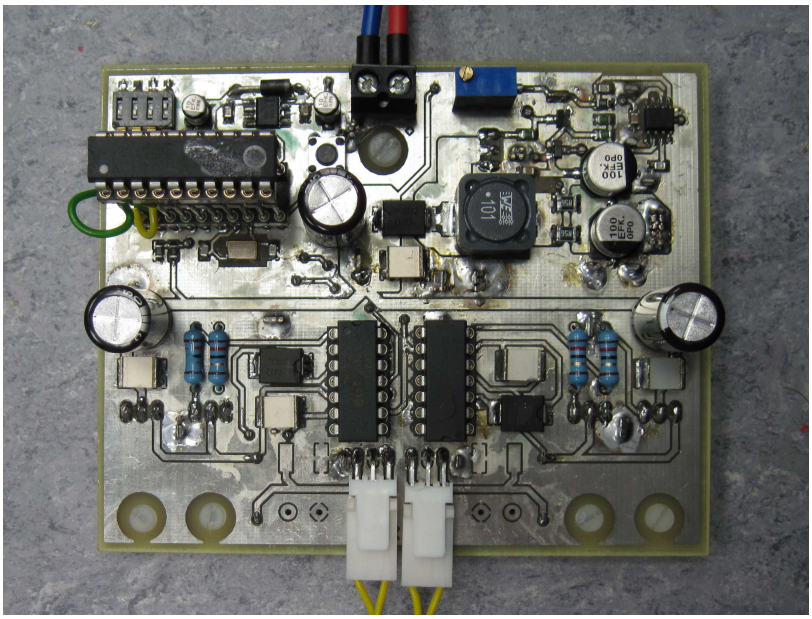


Figure 7.1: Picture of the circuit board of the implemented circuit.

In this chapter the implementation of the circuit is discussed. This incloses the selection of actual parts for the circuit, the laid out PCB and the measured experimental results. In the end the results are evaluated against a commercially available product.

7.1 Part Selection

Hereafter the parts selected for the implementation are discussed. A complete bill of materials can be found in the Appendix. Only the parts relevant to the circuit performance are discussed.

7.1.1 Passives

C3 This is the output capacitor of the boost converter as calculated in Section 6.1. It has to withstand the high output voltage and was selected accordingly. Its value is three times the calculated minimum, which should result in very low voltage ripple at the output.

C11, C12 These capacitors are the capacitive load needed for the crystal *X1* to start oscillating. They are general multilayer ceramic types.

C19 and C26 These are the bootstrap capacitors for the MOSFET driver circuit. There value is lower than calculated in Section 6.2, because the needed high voltage film capacitor was not available with higher capacitances.

C20, C22 and C27, C29 Each high voltage rail in the H-bridge circuit is decoupled using two capacitors. The combination of an aluminium electrolytic capacitor and a metallized film capacitor delivers better performance in terms of lower series resistance and high capacitance. They are the same type as *C3*.

L1 The value for the inductor was determined in Section 6.1. The actual type was selected to match the inductance and current requirements, but also for a small size.

Q1 The crystal is connected to the microcontroller together with load capacitances and deliver the main CPU clock. At 20MHz it is the highest value specified for the ATtiny861. A very compact surface mount part was chosen, to reduce the impact to PCB area.

R3, R4 As the calculated value for the sense resistor $R_{SC} = 0.28\Omega$ was not available for purchase, two 0.56Ω were connected in parallel. The resistors are special in that they have a high power rating of 0.5W despite their small size. This is necessary as they have to withstand the high peak current in the boost converter. Also, chip resistors were chosen as they have a very low inductance, therefore minimizing losses [19].

R5 and R13, R14, R16, R17 These five resistors limit the gate current to the MOSFETs. They are calculate to deliver the maximum current to the gate the respective driver circuit is capable of.

S2 This 4-way switch block is connected to the microcontroller and can be used to alter parameters like the frequency of the PWM generation. A surface mount part was chosen for its small size.

7.1.2 Diodes

D1 and D3, D4 The diodes are those that were selected in Section 6.2 and Section 6.1 (Diodes Inc. MURS320).

7.1.3 Integrated Circuits

IC1 This is the microcontroller Atmel ATtiny861 (see Section 6.3).

IC2 As the microcontroller needs a stable 5V power supply, the 78L05 linear voltage regulator was added to the circuit. It drops down the 12V input voltage to a regulated 5V output.

U1 This IC is the boost converter control circuit MC34063. It is available from various manufacturers with the same specifications, however a Texas Instruments part was chosen as for its low price.

U2, U3 These are the International Rectifier IR2110 half-bridge gate driver circuits as discussed in Section 6.2. Through-hole parts were used, even though they need more PCB area. They offer the advantage of being easy to replace in case of failure.

7.1.4 Transistors

M1 and M2, M3, M4, M5 Five identical International Rectifier IRFB4020PbF MOSFETs were integrated in the circuit as these were chosen in Section 6.1 and Section 6.2. They come in the relatively large TO-220AB package.

T1, T2 As discussed in Section 6.1 a pair of complimentary bipolar junction transistors were used as a gate driver. The used NXP BC807-40 and BC817-40 come in the very small SOT-23 package and therefore need little PCB space. They are very cheap, too.

7.2 PCB Layout

The actual PCB artwork for the DC-AC inverter is shown in Figure 7.2. On the top and bottom layer a ground plane was used to supply a low impedance ground return path for all ground connections in the circuit. To ensure as short as possible ground paths the top and bottom ground planes were interconnected with many vias, especially in critical areas like the ground connections of the decoupling capacitors. The circuit board measures 100mm × 80mm in size. Some trade-offs had to be accepted, as the PCB was made in-house and plated through holes were not possible. Therefore all vias had to be contacted using short pieces of copper wire soldered to both sides of the board. This is the reason why most components were placed on the top layer of the PCB.

For the high-current paths in the boost converter circuit copper planes were used instead of tracks. They are at least 3mm wide and should be able to carry over 4A of current safely [19]. The smallest PCB track size in the circuit is 0.4064mm due to the design rules for the in-house manufacturing process. These tracks should still be able to carry over 1A of current, therefore their impedance is negligible [19].

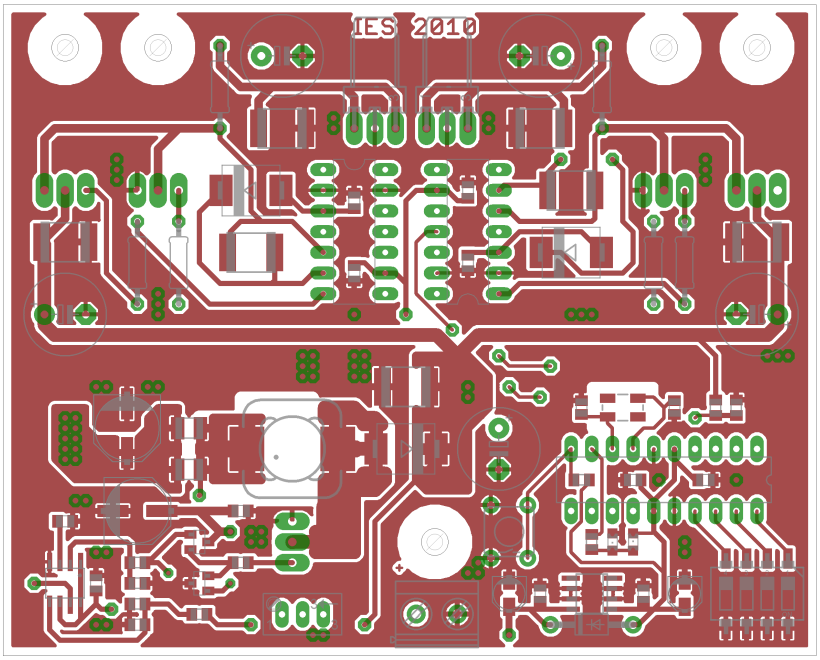
7.3 Experimental Results

The performance of the implemented circuit was measured using the test circuit pictured in Figure 7.3. The DC-DC converter was examined separately, as this data is needed for the evaluation of the boost converter circuit.

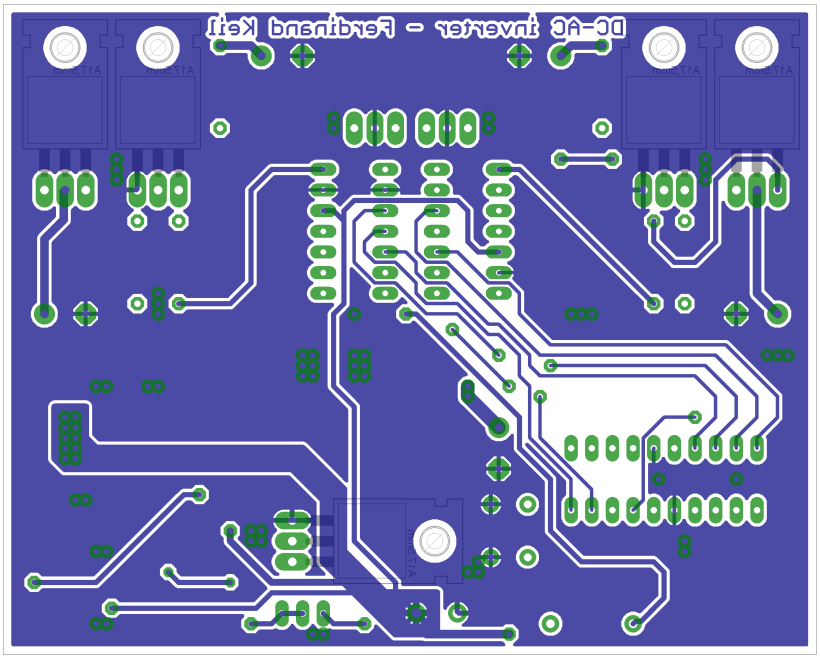
7.3.1 DC-DC Converter

Several separate measurement were conducted for the DC-DC converter part of the implemented circuit. First of the efficiency was measured for an output voltage of $V_{OUT} = 60\text{V}$ and an output current of $I_{OUT} = 100\text{mA}$. This resulted in a measured power efficiency of $\eta = 77.43\%$. In the result the measured power efficiency of the actual circuit is lower than in the simulation. The reasons are the non-zero circuit track impedance, the losses in the capacitors and the differences between the modelled components and their real counterparts.

The ripple voltage at the output and the ramp up time were also measured. Figure 7.4 shows that the ripple voltage in the actual circuit is more than two times higher than in the simulation. For the actual circuit a ripple voltage of $V_{ripple(pp),meas} = 190\text{mV}$ was measured, while the value in the simulation was at $V_{ripple(pp),sim} = 89\text{mV}$. The reason is the series resistance of the output capacitor.



(a) Top layer



(b) Bottom layer

Figure 7.2: The PCB artwork for the DC-AC inverter circuit.

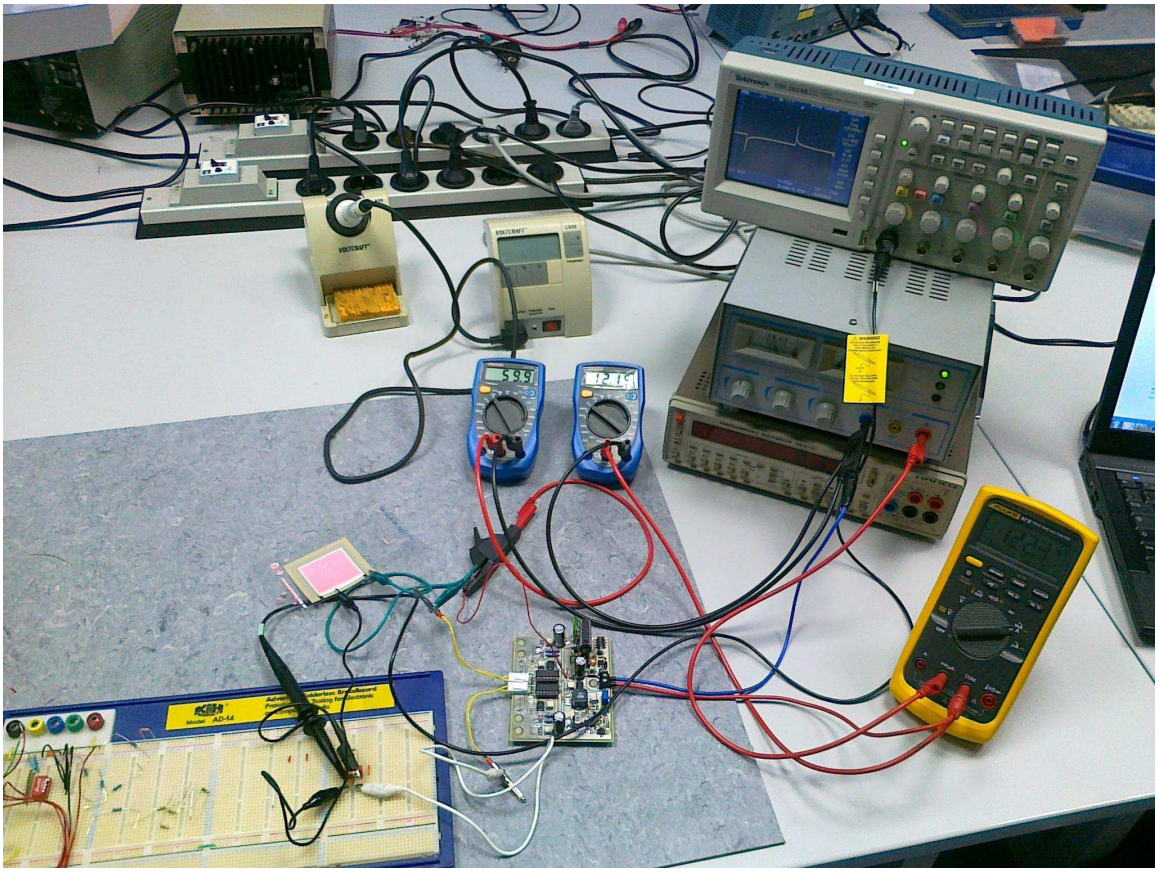


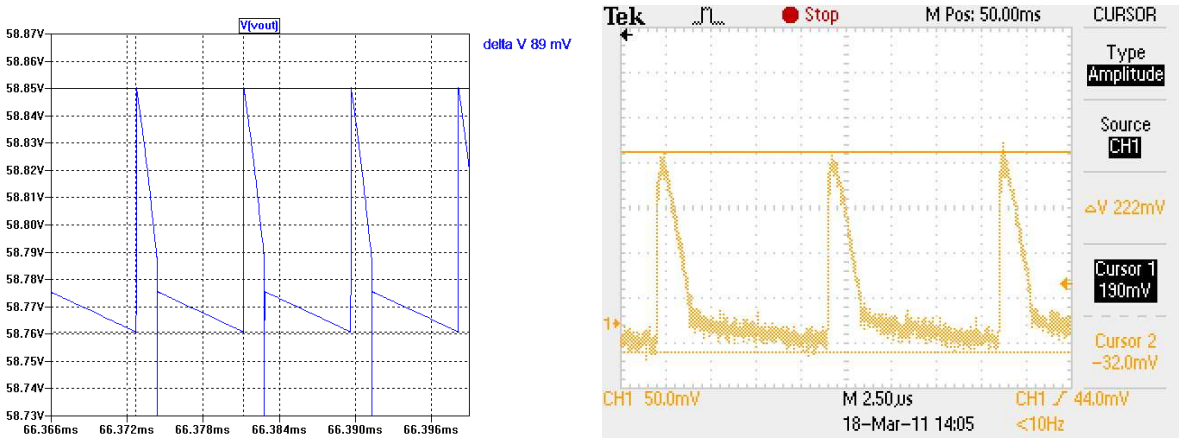
Figure 7.3: Picture of the test circuit used to characterize the implemented circuit.

It causes losses in the capacitor but also lets it react slower to high frequency current ripple.

The ramp-up time of the real circuit is also longer than predicted in the simulation. In the simulation the output voltage of the boost converter took only $t_{ramp-up,sim} =$ 61ms to become stable, while a value of $t_{ramp-up,meas} = 101$ms was measured for the real circuit. This can be explained with leakage currents in the output capacitors and the non-zero impedance of the circuit tracks and cables connecting the converter to the voltage source. The ramp-up waveforms are shown in Figure 7.5.

7.3.2 DC-AC Inverter Circuit

To calculate the overall power efficiency of the circuit, the input voltage, input current, output voltage and output current waveform were measured. The resulting output current waveform is shown in Figure 7.6. The efficiency was measured for several



(a) Simulation (b) Real circuit

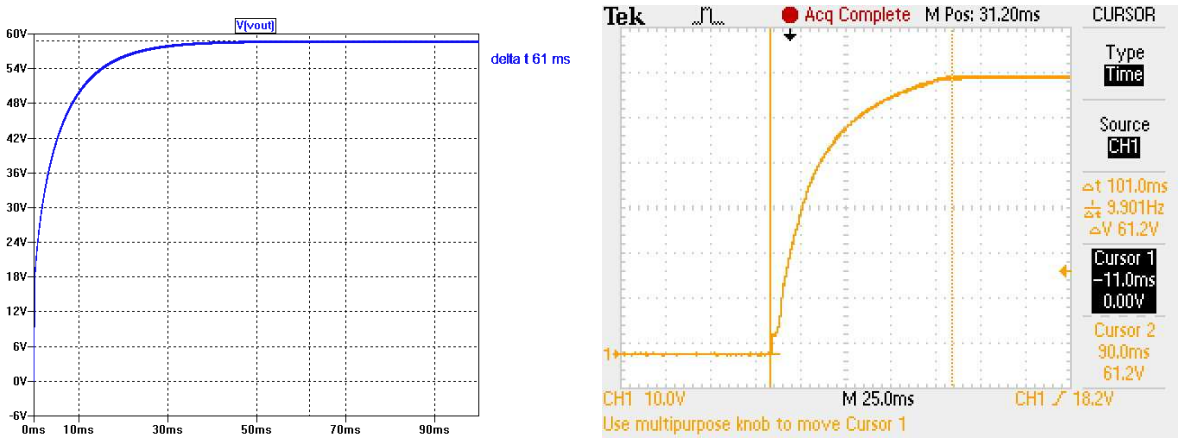
Figure 7.4: Output voltage ripple in the real circuit and the simulation.

different loads. The results are listed in Table 7.1.

Load	**Efficiency**
EL Panel	35.48%
Electrical Model 1 ($R_{ser} = 100\Omega$, $R_{par} = 10\text{k}\Omega$, $C = 15\text{nF}$)	69.66%
Electrical Model 2 ($R_{ser} = 400\Omega$, $R_{par} = 10\text{k}\Omega$, $C = 15\text{nF}$)	37.17%
Resistive Load $R_{load} = 450\Omega$	81.53%

Table 7.1: Measured results for the DC-AC inverter and different loads.

Even though the values for the electrical model 1 were taken from Table 3.1, the efficiency is much higher than for the actual EL panel. This is because the electrical model 1 has a higher power consumption than the EL panel. The model determined in Section 3.3 therefore is not accurate. The series resistance of the equivalent circuit was then increased until the power consumption matched the one for the EL panel. The efficieny was measured again with $R_{ser} = 400\Omega$ and resulted in a power efficiency that is approximately the same as for the EL panel. The measured value of 35.48% efficiency for the EL panel is correct, but much lower than expected. The reason for this large difference, is that the DC-AC inverter circuit has a relatively high quiescent power consumption. The models used in the simulation did not include the power consumption of the integrated circuits. Even though the microcontroller's power consumption was tried to model, it was measured to be more than twice the value used in the simulation. Because of the quiescent power consumption being not dependent on the output power, the power efficiency of the circuit is worst at very low output powers. To prove this, the efficiency was measured again with a resistive



(a) Simulation (b) Real circuit

Figure 7.5: Ramp-up time in the real circuit and the simulation.

load of 450Ω connected to the output of the inverter circuit. The measured efficiency reached 81.53%, which is close to the simulated result of 88.53%. This proves the assumption of a relatively high quiescent power consumption.

7.4 Evaluation

This work	77.43%	@ $V_{OUT} = 60\text{V}$, $I_{OUT} = 100\text{mA}$
Texas Instruments TPS61085	90%	@ $f = 650\text{kHz}$, $L = 6.8\mu\text{H}$, $I = 150\text{mA}$, $V_{in} = 3.3\text{V}$, $V_S = 12\text{V}$
Texas Instruments TPS40210	$\sim 90\%$	@ $I_{LOAD} \approx 150\text{mA}$, $V_{IN} = 8\text{V}$
aimtec AM2F-0524SZ	68%	@ $V_{IN} = 5\text{V}$, $V_{OUT} = 24\text{V}$, $I_{OUT} = 83\text{mA}$

Table 7.2: Comparison of the efficiency of the boost converter part to other existing designs.

As mentioned in Section 6.5, no data on the efficiency of other DC-AC inverter design was available. Therefore only the DC-DC converter part can be compared to other commercially available products. The results are shown in Table 7.2. Compared to the Texas Instruments devices the designed boost converter circuit is more than twelve percent less efficient. However, compared to the integrated DC-DC converter module it still performs superior. The DC-DC converter's overall performance can be judged as relatively high efficiency.

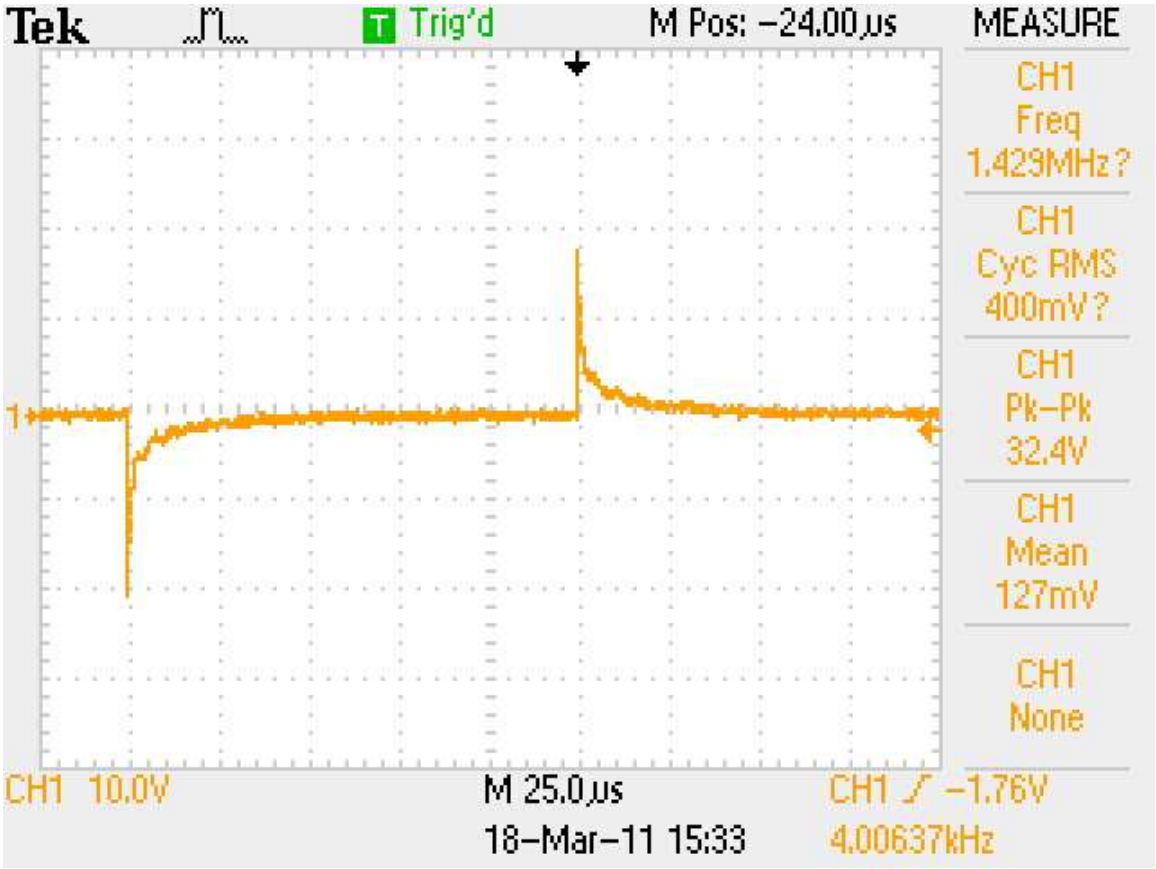


Figure 7.6: Output current waveform of the DC-AC inverter with an EL panel as load.

8 Conclusion and Outlook

In this chapter a conclusion is reached and an outlook to future work given.

8.1 Conclusion

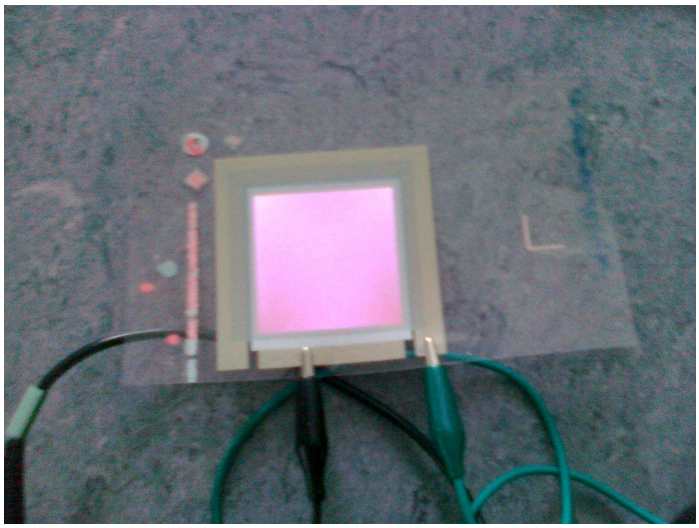


Figure 8.1: Picture of an EL panel glowing while connected to the implemented circuit.

After explaining the operating principle of the EL panel and to parameterizing an equivalent elictrical model, several different DC-DC and DC-AC converter topologies were introduced. The boost converter topology connected to an H-bridge was chosen as the solution that fits at best. The basic operation of the boost converter were discussed and all important design formulas were derived. After a control circuit was chosen the component values for the converter were calculated and optimized. For the H-bridge circuit an integrated gate driver circuit was selected and the values of the surrounding components were calculated. The H-bridge circuit was also optimized. The H-bridge was connected to the boost converter circuit and the overall

system power efficiency was calculated from the simulation's results. The results were evaluated against commercially available devices.

The circuit was then entered in CAD (Computer Aided Design) software and a PCB layout was made. The choice of actual components was explained and the parts ordered from an electronic parts distributor. The layout artwork was sent to an in-house PCB manufacturer and the ordered components were soldered to the board. A control program for the used microcontroller was created and programmed to the controller's program memory. A test circuit was built and the circuits performance was measured. The measured results were again evaluated against commercial designs.

In the end a working circuit was achieved and EL panels connected to it indeed glow, as shown in Figure 8.1. Not all design specifications established in Section 2.2 were met. Table 8.1 compares the achieved results with these design specifications. The dimming of the EL panel is not possible yet, but can be implemented with an update of the microcontroller's control program. However, the frequency of the output waveform can already be configured via switches, which also changes the panel's brightness.

The goal of a power efficiency above 80% was not met when the circuit was connected to the EL panel. The reason is the high quiescent power consumption of the circuit. The efficiency improves for higher loads. As EL panels of greater area present a larger load, it is likely that the circuit performs better when connected to one of those.

DC input voltage $\leq$ 12V	yes (= 12V)
Variable AC output voltage $\geq 120V_{peak-peak}$	yes
Compact design	no
Low audible noise emission	yes
High efficiency $\geq$ 80%	no
Dimming of EL panel	yes (not implemented yet)

Table 8.1: Comparison of the design specification to the achieved results.

8.2 Outlook

The circuit can still be optimized in several ways. First of all the quiescent power consumption of the circuit could be reduced, for example by using power saving features of the employed microcontroller. Also the circuit could be made more compact in terms of PCB area. Using a four layer circuit board with plated through holes and placing the components on both sides of the circuit, the board size could be reduced

at least 25%. The analog-digital converter of the microcontroller could be used for monitoring the output voltage. A short-circuit protection could be built on top of this.

Bibliography

[1] V. Arancio and J. R. Dorfman. Improved characterisation of electromluminescent lamps through environmental and electrical stress testing, 2003. `http://www2.dupont.com/MCM/en_US/PDF/techpapers/ELPAPER.pdf` [Online; accessed 28-Feb-2011].

[2] Atmel Corporation. Attiny261/461/861 datasheet, 2009. Rev. 2588C - 10/09.

[3] J. A. Hart, S. A. Lenway, and T. Murtha. A history of electroluminescent displays, 1999. `http://www.indiana.edu/~hightech/fpd/papers/ELDs.html` [Online; accessed 28-Feb-2011].

[4] P. Horowitz and W. Hill. *The Art of Electronics*. Cambridge University Press, New York, NY, USA, 1989.

[5] R. C. Jaeger and T. N. Blalock. *Microelectronic Circuit Design*. McGraw-Hill International, New York, NY, USA, third edition edition, 2008.

[6] NXP. Bc807 datasheet, 2009. Rev. 06 - 17 November 2009.

[7] NXP. Bc817 datasheet, 2009. Rev. 06 - 17 November 2009.

[8] Y. A. Ono. *Electroluminescent Displays*. World Scientific Publishing, Singapore, 1995.

[9] Panasonic. Aluminium electrolytic capacitor series ee type a datasheet, 2008. Apr. 2008.

[10] A. I. Pressman, K. Billings, and T. Morey. *Switching Power Suppy Design*. McGraw-Hill, New York, NY, USA, third edition edition, 2009.

[11] International Rectifier. Ir2110 datasheet, 2005. Rev. U.

[12] International Rectifier. Irfb4020pbf datasheet, 2006. 03/03/06.

[13] International Rectifier. Application note an-978 hv floating mos-gate driver ics, 2007. Rev. D - 3/23/2007.

[14] H. M. Sauer, C. Ranfeld, and E. Dörsam. An investigation of the screen printing process for electroluminescent panels and the influence of printing and operation parameters on the performance of the panels. In *Proceedings LOPE-C*, 2010.

[15] ON Semiconductor. An920/d theory and applications of the mc34063 and ua78s40 switching regulator control circuits, 2006. May, 2006 - Rev. 5.

[16] ON Semiconductor. Mc34063a datasheet, 2007. February 2007 - Rev. 19.

[17] Linear Technology. Ltspice iv, 2011. `http://www.linear.com/designtools/software/` [Online; accessed 13-Mar-2011].

[18] Wikipedia. Electroluminescence — wikipedia, the free encyclopedia, 2011. `http://en.wikipedia.org/w/index.php?title=Electroluminescence&oldid=408143145` [Online; accessed 28-Feb-2011].

[19] Tim Williams. *The Circuit Designer's Companion*. Elsevier, Oxford, GB, 2005.

A Source Code

Listing A.1: Header File - main.h

```
1  /*
2    bachelor thesis
3    inverter for EL displays
4
5    main.c - header
6  */
7
8  /* definitions */
9
10 #ifndef F_CPU
11   #define F_CPU 20000000UL
12   #warning Kein F_CPU definiert
13 #endif
14
15
16 /* includes */
17
18 #include <stdint.h>
19 #include <avr/io.h>
20 #include <avr/interrupt.h>
21 #include <util/delay.h>
22
23
24 /* variables */
25
26 // non-linear
27 // 500Hz steps from 500 - 4000Hz
28 // 2kHz steps from 4 - 20kHz
29 struct freq {
30   uint8_t prescaler;
31   uint8_t top;
32   uint8_t compare;
33 } freqtab[] = {
```

```
34    {0X08, 156,  78}, //  0
35    {0x08,  78,  39}, //  1
36    {0x08,  52,  26}, //  2
37    {0x07,  78,  39}, //  3
38    {0x06, 125,  63}, //  4
39    {0x06, 104,  52}, //  5
40    {0x05, 179,  90}, //  6
41    {0x06,  78,  39}, //  7
42    {0x06,  52,  26}, //  8
43    {0x05,  78,  39}, //  9
44    {0x04, 125,  63}, // 10
45    {0x04, 104,  52}, // 11
46    {0x03, 179,  90}, // 12
47    {0x04,  78,  39}, // 13
48    {0x03, 139,  70}, // 14
49    {0x02, 250, 125}  // 15
50 };
51
52 // Switch state
53 volatile uint8_t switch_state;
54
55
56 /* functions */
57
58 void delay(void);
59 void init(void);
60 void loop(void);
```

Listing A.2: Header File - main.c

```
1 /*
2   bachelor thesis
3   inverter for EL displays
4
5   main.c
6 */
7
8 #include "main.h"
9
10 void init(void) {
11   // Port setup
12   // Port A
13   // PA[0:5] inputs, PA[6:7] outputs
```

```
14  DDRA = (1<<PA7) | (1<<PA6);
15  // PA[0:3] internal pullups on, PA[6:7] high
16  PORTA = (1<<PA7) | (1<<PA6) | (1<<PA3) | (1<<PA2) | (1<<PA1
        ) | (1<<PA0);
17
18  // Port B
19  // PB[0:5] outputs, PB6 input
20  DDRB = 0xFF & ~(1<<PB6);
21  // PB[0:7] low
22  PORTB = 0;
23
24
25  // Timer0 setup
26  // Compare match mode
27  TCCR0A = (1<<WGM00);
28  // Prescaler clk/1024
29  TCCR0B = (1<<CS02) | (1<<CS00);
30  // Output compare match every 10ms
31  OCR0A = 196;
32  // Interrupt on output compare match A
33  TIMSK = (1<<OCIE0A);
34
35
36  // Timer1 setup
37  // Channel 1A and 1B PWM, regular and inverted output
        connected
38  TCCR1A = (1<<PWM1B) | (1<<PWM1A) | (1<<COM1B0) | (1<<COM1A0
        );
39  // Timer stopped, dead time prescaler clk/4
40  TCCR1B = (1<<DTPS11) | (1<<DTPS10);
41  // Phase and frequency correct PWM mode
42  TCCR1D = (1<<WGM10);
43  // Dead time counter value
44  DT1 = 0xFF;
45  // Standard values for the output compare registers
46  OCR1C = 0;
47  OCR1A = 0;
48  OCR1B = 0;
49
50
51  // Enable interrupts globally
52  sei();
```

```
53
54
55    // Turn red LED on
56    PORTB |= (1<<PB6);
57    DDRB |= (1<<PB6);
58  }
59
60  void loop(void) {
61    static uint8_t prev_state;
62    uint8_t n;
63
64
65    // Check if switch state has changed
66    if (switch_state != prev_state) {
67      // If true, load registers with new values
68      PORTA |= (1<<PA7) | (1<<PA6);    // turn H-bridge off
69      prev_state = switch_state;
70      n = switch_state & 0x0F;
71      TCCR1B = (TCCR1B & 0xF0) | (freqtab[n].prescaler & 0x0F);
72      OCR1C = freqtab[n].top;
73      OCR1A = freqtab[n].compare;
74      OCR1B = freqtab[n].compare;
75      PORTA &= ~((1<<PA7) | (1<<PA6));  // turn H-bridge on
76    }
77  }
78
79  ISR( TIMER0_COMPA_vect ) {
80    /*
81      SOURCE:
82      Debouncing 8 Keys
83      Peter Dannegger
84      http://www.mikrocontroller.net/articles/Entprellung
85    */
86
87    static uint8_t ct0, ct1;
88    uint8_t i;
89
90    i = switch_state ^ ~PINA;    // key changed?
91    ct0 = ~( ct0 & i);          // reset or count ct0
92    ct1 = ct0 ^ (ct1 & i);       // reset or count ct1
93    i &= ct0 & ct1;            // count until roll over?
94    switch_state ^= i;          // then toggle debounced state
```

```
95 }
96
97 int main(void) {
98
99     init();
100
101     for (;;) {
102         loop();
103     }
104
105     return 0;
106 }
```

B Implementation Schematic

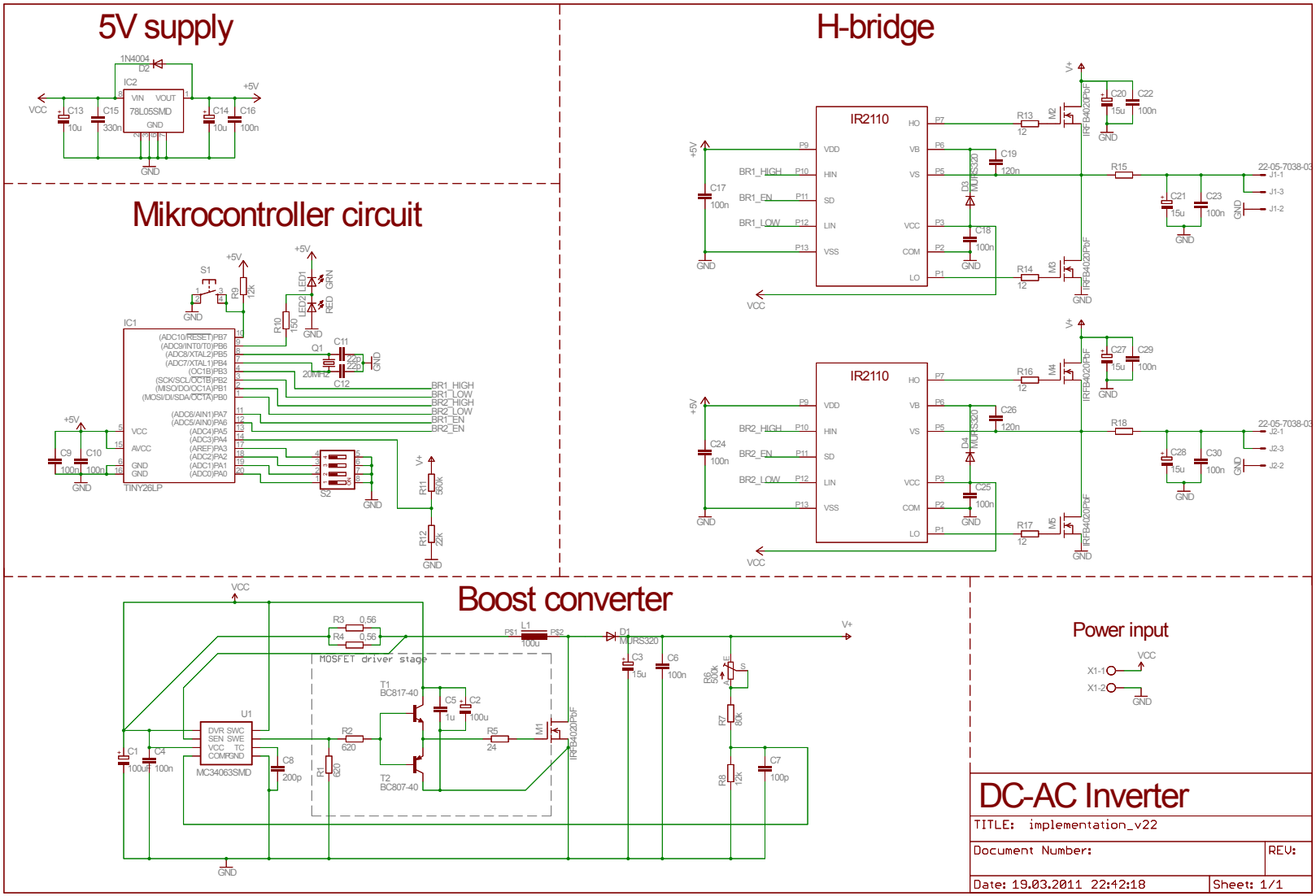


Figure B.1: Schematic diagram of the implemented circuit.

C Bill of Materials

Part	Value	Farnell SKU	Manufacturer
C1	100u	9695770	PANASONIC
C2	100u	9695770	PANASONIC
C3	15u	1673477	PANASONIC
C4	100n	1414664	KEMET
C5	1u	1845770	MURATA
C6	100n	1744866	PANASONIC
C7	220p	1414679	KEMET
C8	220p	1414679	KEMET
C9	100n	1414664	KEMET
C10	100n	1414664	KEMET
C11	22p	1362555	YAGEO (PHYCOMP)
C12	22p	1362555	YAGEO (PHYCOMP)
C13	10u	9695729	PANASONIC
C14	10u	9695729	PANASONIC
C15	330n	1833878	AVX
C16	100n	1414664	KEMET
C17	100n	1414664	KEMET
C18	100n	1414664	KEMET
C19	120n	1744867	PANASONIC
C20	15u	1673477	PANASONIC
C21			
C22	100n	1744866	PANASONIC
C23			
C24	100n	1414664	KEMET
C25	100n	1414664	KEMET
C26	120n	1744867	PANASONIC
C27	15u	1673477	PANASONIC
C28			
C29	100n	1744866	PANASONIC
C30			
D1	MURS320	9557555	ON SEMICONDUCTOR
D2	1N4004	1651084	ON SEMICONDUCTOR

D3	MURS320	9557555	ON SEMICONDUCTOR
D4	MURS320	9557555	ON SEMICONDUCTOR
IC1	TINY26LP	1841627	ATMEL
IC2	78L05SMD	1652342	ON SEMICONDUCTOR
J1	22-05-7038-03	9731610	MOLEX
J2	22-05-7038-03	9731610	MOLEX
J1-C		143127	MOLEX
J2-C		143127	MOLEX
J12-C		9773789	MOLEX
L1	100u	1635948	WUERTH ELEKTRONIK
LED1	GRN	1686074	KINGBRIGHT
LED2	RED	1686066	KINGBRIGHT
M1	IRFB4020PbF	1436954	INTERNATIONAL RECTIFIER
M2	IRFB4020PbF	1436954	INTERNATIONAL RECTIFIER
M3	IRFB4020PbF	1436954	INTERNATIONAL RECTIFIER
M4	IRFB4020PbF	1436954	INTERNATIONAL RECTIFIER
M5	IRFB4020PbF	1436954	INTERNATIONAL RECTIFIER
Q1	20MHz	1611815	ABRACON
R1	620	1400314	KOA
R2	620	1400314	KOA
R3	0,56	1717929	PANASONIC
R4	0,56	1717929	PANASONIC
R5	24	1400276	KOA
R6	500k	9608672	VISHAY SPECTROL
R7	80k	1100327	WELWYN
R8	12k	1100321	WELWYN
R9	12k	1100321	WELWYN
R10	620	1400314	KOA
R11	560k	1100332	WELWYN
R12	22k	1099809	WELWYN
R13	12	9339922	MULTICOMP
R14	12	9339922	MULTICOMP
R15			
R16	12	9339922	MULTICOMP
R17	12	9339922	MULTICOMP
R18			
S1			
S2		1524007	MULTICOMP
T1	BC817-40	1081225	NXP

T2	BC807-40	1081222	NXP
U1	MC34063AD	1053582	TEXAS INSTRUMENTS
U2	IR2110-SMD	8638845	INTERNATIONAL RECTIFIER
U3	IR2110-SMD	8638845	INTERNATIONAL RECTIFIER
X1	MKDSN1,5/2-5,08	1131855	WEIDMULLER